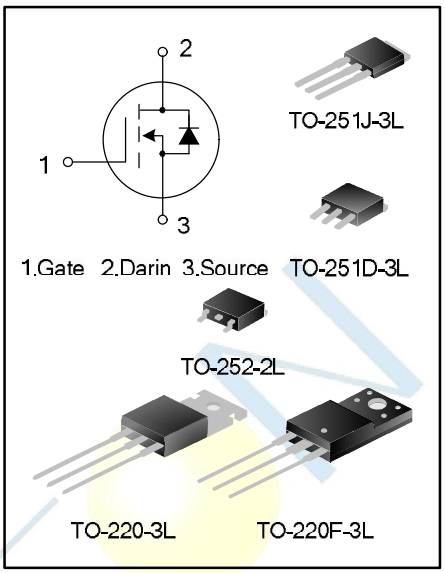
4A, 650V N-CHANNEL MOSFET

GENERAL DESCRIPTION

This power mosfet is an N-channel enhancement mode power MOS field effect transistor which is produced using Hi-semicon proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

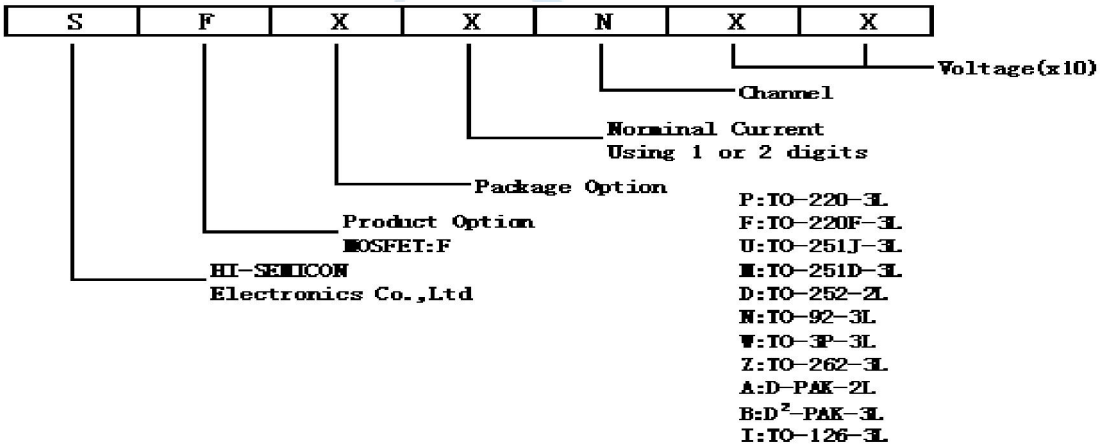
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 4A,650V, $R_{DS(on)(typ)}$=2.3Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SFP4N65	TO-220-3L	SFP4N65	Pb free	Tube
SFF4N65	TO-220F-3L	SFF4N65	Pb free	Tube
SFU4N65	TO-251J-3L	SFU4N65	Pb free	Tube
SFM4N65	TO-251D-3L	SFU4N65	Pb free	Tube
SFD4N65	TO-252-2L	SFD4N65	Pb free	Tape & Reel

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Ratings				Unit
			SFP4N65	SFF4N65	SFM/D4N65	SFU4N65	
Drain-Source Voltage		V_{DS}	650				V
Gate-Source Voltage		V_{GS}	±30				V
Drain Current	T_C=25°C	I_D	4.0				A
	T_C=100°C		2.8				
Drain Current Pulsed		I_{DM}	16				A
Power Dissipation(T_C=25°C)		P_D	100	33	77	79	W
-Derate above 25°C			0.80	0.26	0.62	0.63	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	202				mJ
Operation Junction Temperature Range		T_J	-55～+150				°C
Storage Temperature Range		T_{stg}	-55～+150				°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings				Unit
		SFP4N65	SFF4N65	SFM/D4N65	SFU4N65	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.25	3.79	1.62	1.58	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	120	110	110	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=2A	--	2.3	2.7	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ	--	464	--	pF
Output Capacitance	C_{oss}		--	54	--	
Reverse Transfer Capacitance	C_{rss}		--	1.32	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V,I_D=4.0A, R_G=25Ω (Note 2,3)	--	16.6	--	ns
Turn-on Rise Time	t_r		--	37.33	--	
Turn-off Delay Time	$t_{d(off)}$		--	18.0	--	
Turn-off Fall Time	t_f		--	19.2	--	
Total Gate Charge	Q_g	V_{DS}=520V,I_D=4.0A, V_{GS}=10V (Note 2,3)	--	8.03	--	nC
Gate-Source Charge	Q_{gs}		--	2.57	--	
Gate-Drain Charge	Q_{gd}		--	3.03	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	4.0	A
Pulsed Source Current	I_{SM}		--	--	16	
Diode Forward Voltage	V_{SD}	I_S=4.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=4.0A,V_{GS}=0V, dI_F/dt=100A/μs	--	455.23	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.01	--	μC

Notes:

1. L=30mH,I_{AS}=3.36A,V_{DD}=150V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

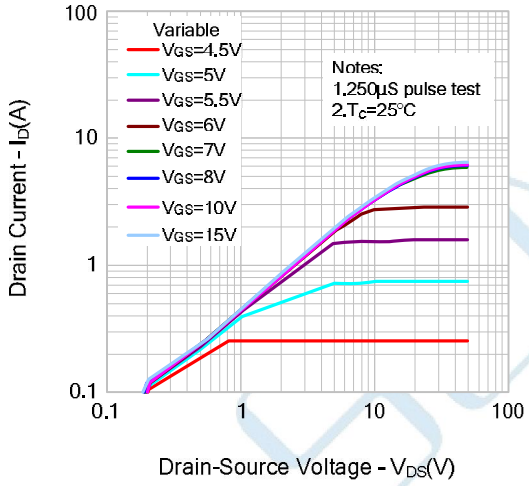


Figure 2. Transfer Characteristics

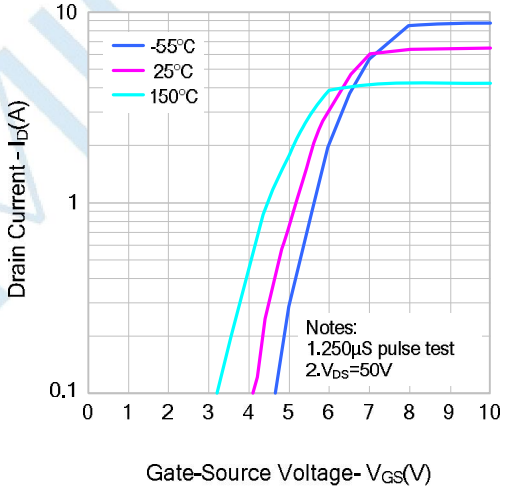


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

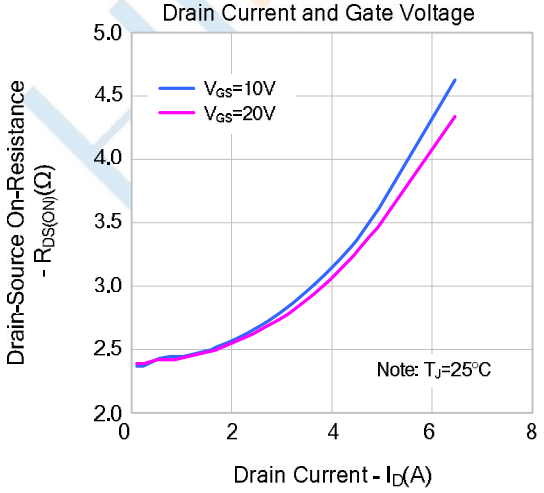
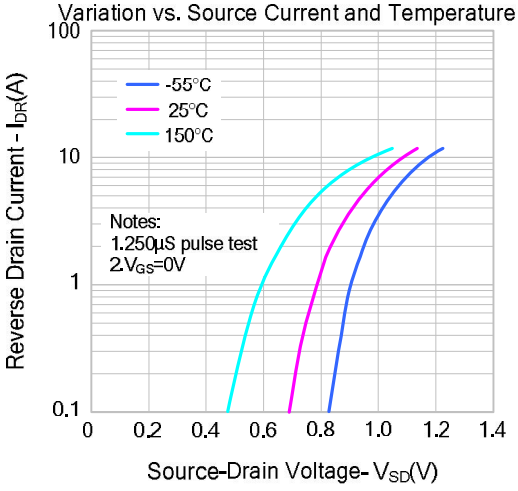


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL CHARACTERISTICS(continued)

Figure 5. Capacitance Characteristics

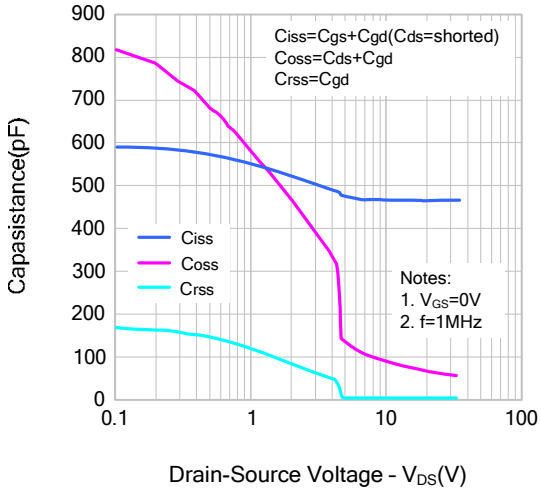


Figure 6. Gate Charge Characteristics

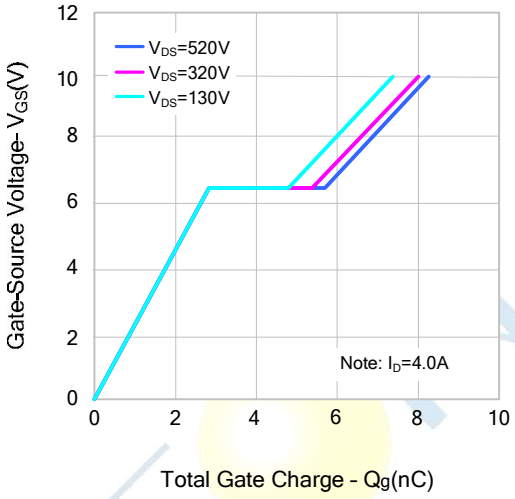


Figure 7. Breakdown Voltage Variation vs. Temperature

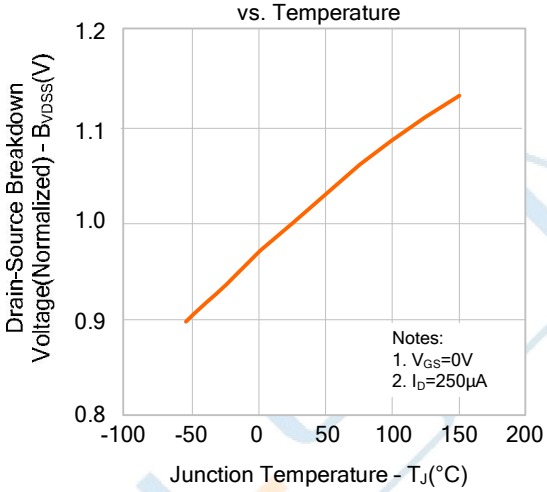


Figure 8. On-resistance Variation vs. Temperature

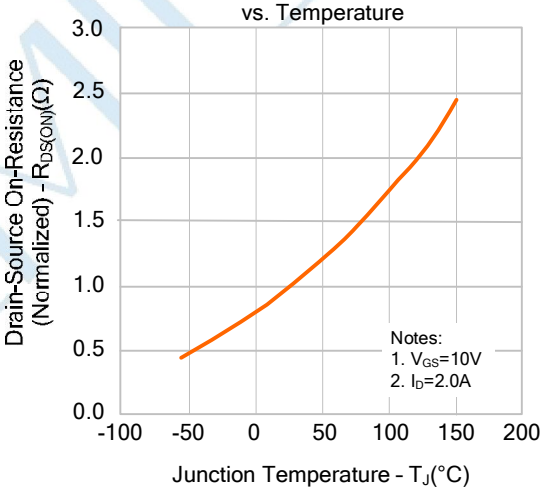


Figure 9-1. Max. Safe Operating Area(SFP4N65)

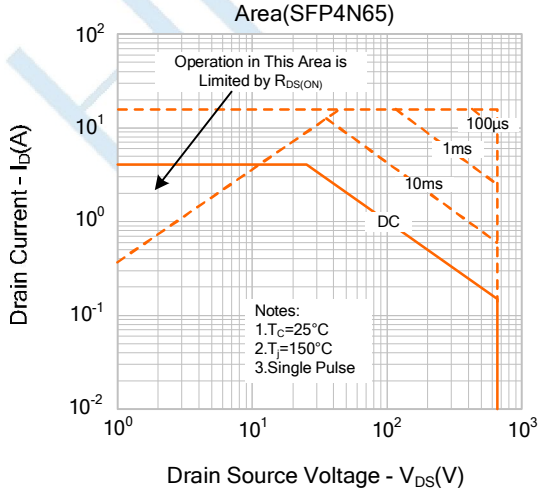
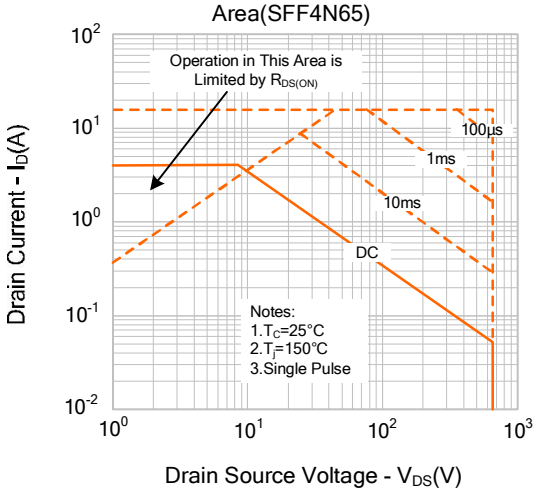


Figure 9-2. Max. Safe Operating Area(SFF4N65)



TYPICAL CHARACTERISTICS(continued)

Figure 9-3. Max. Safe Operating Area (SFM/D4N65) ,

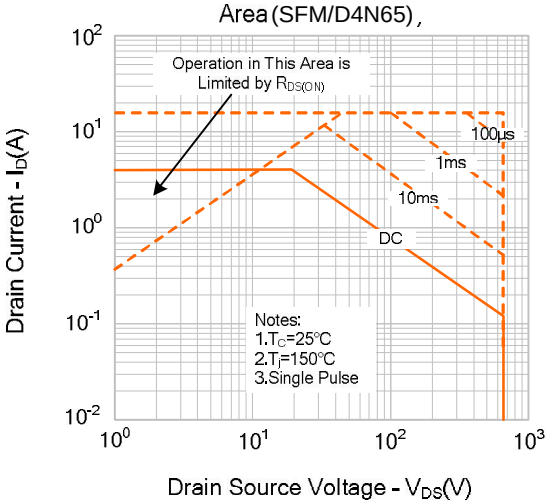


Figure 9-4. Max. Safe Operating Area(SFU4N65)

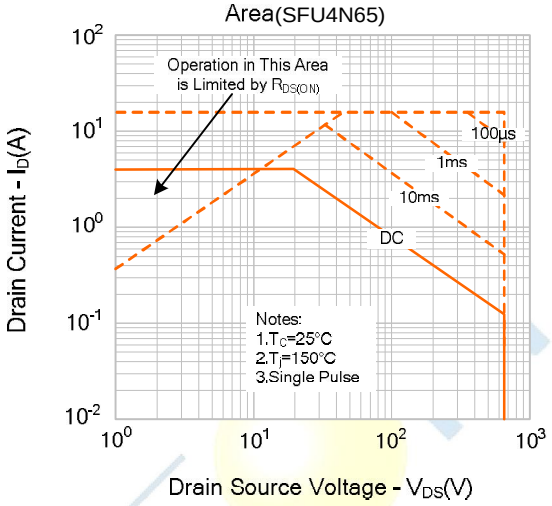
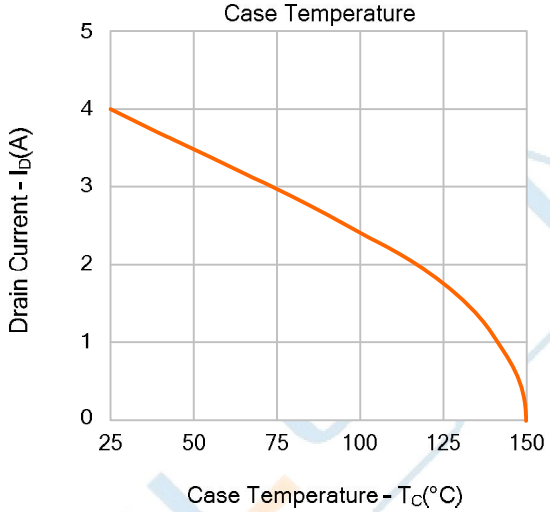
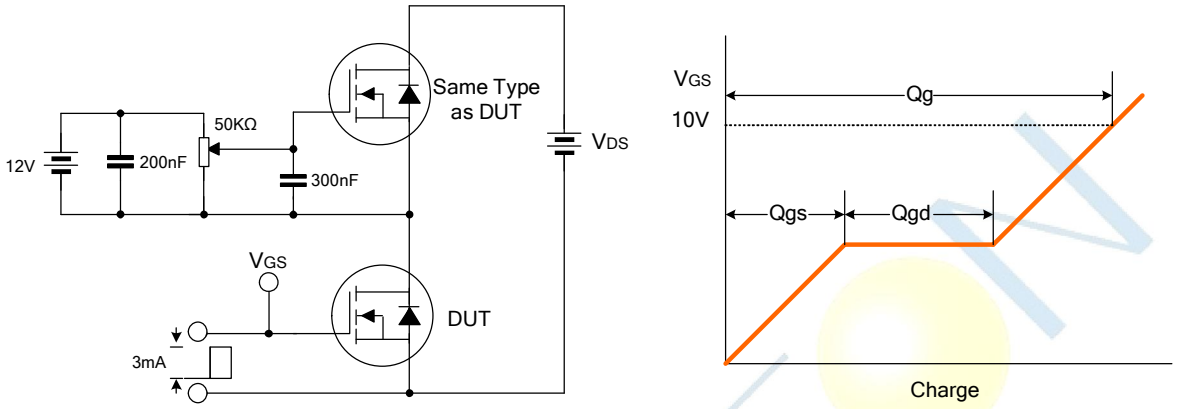


Figure 10. Maximum Drain Current vs. Case Temperature

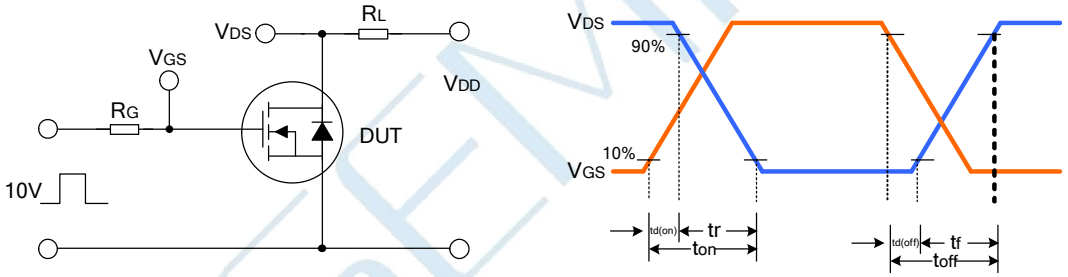


TYPICAL TEST CIRCUIT

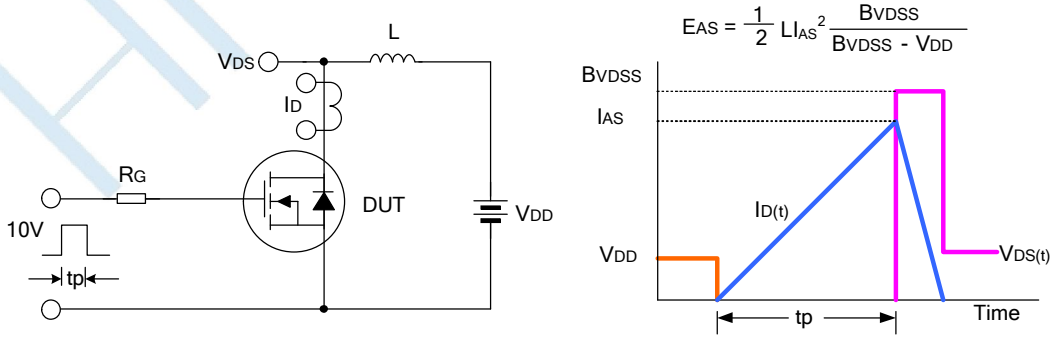
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

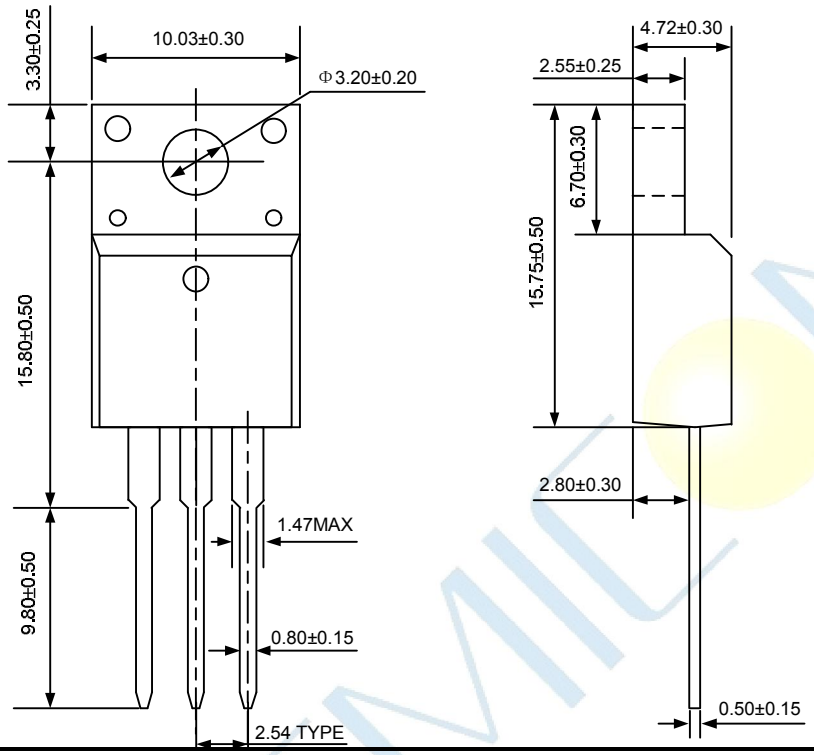


Unclamped Inductive Switching Test Circuit & Waveform

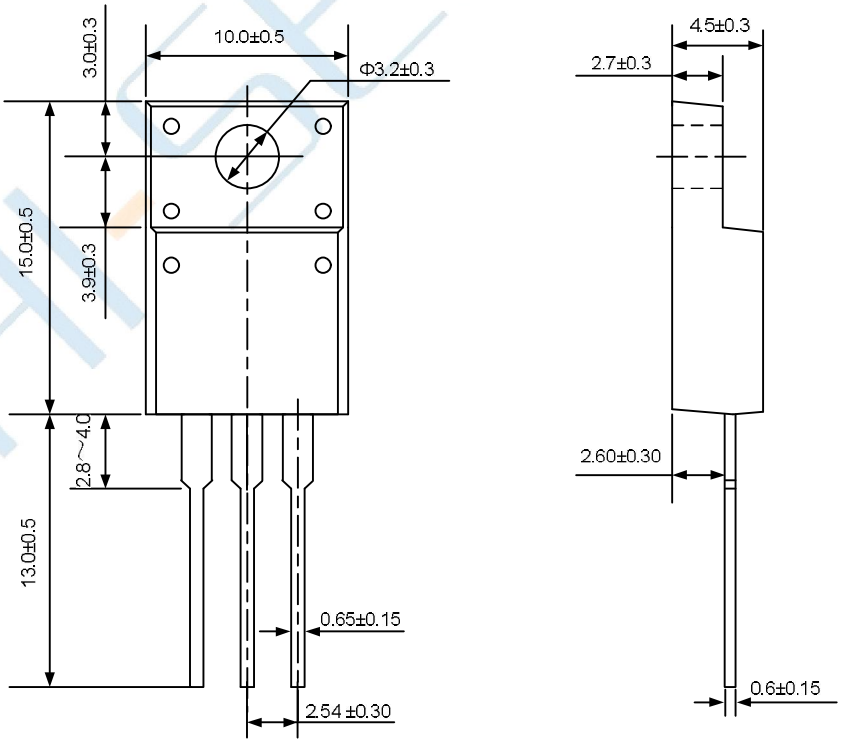


PACKAGE OUTLINE

TO-220F-3L(1) **UNIT: mm**

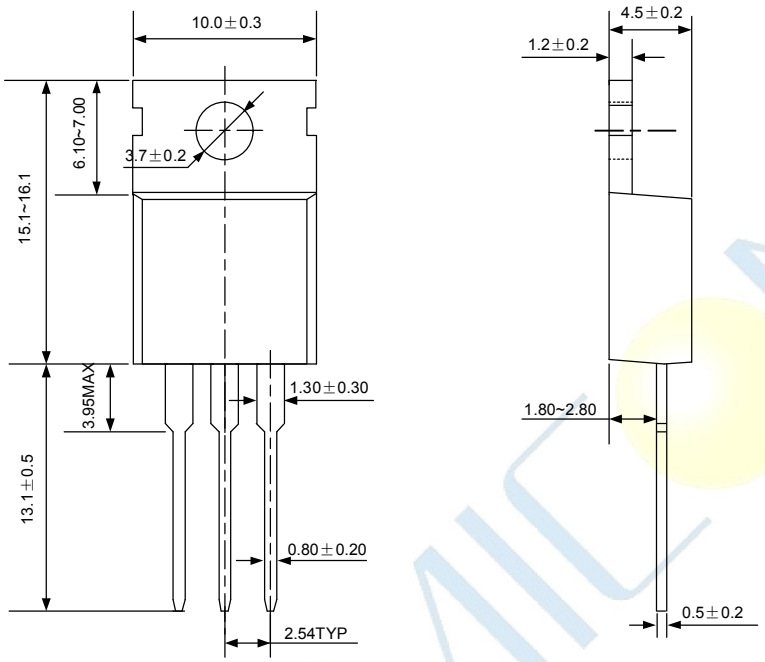


TO-220F-3L(2) **UNIT: mm**

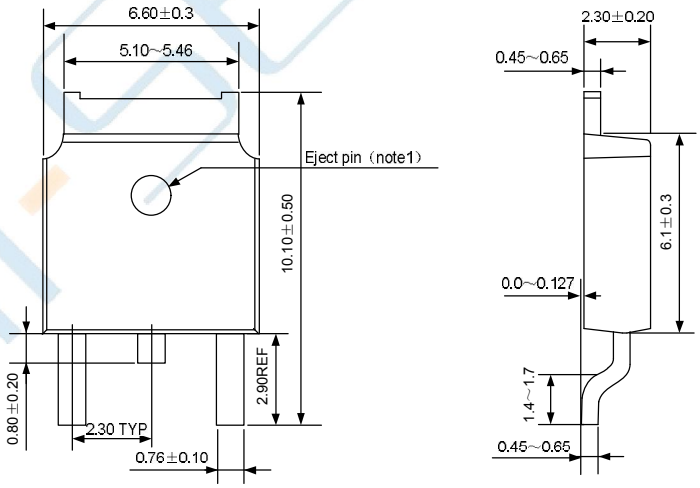


PACKAGE OUTLINE (continued)

TO-220-3L **UNIT: mm**



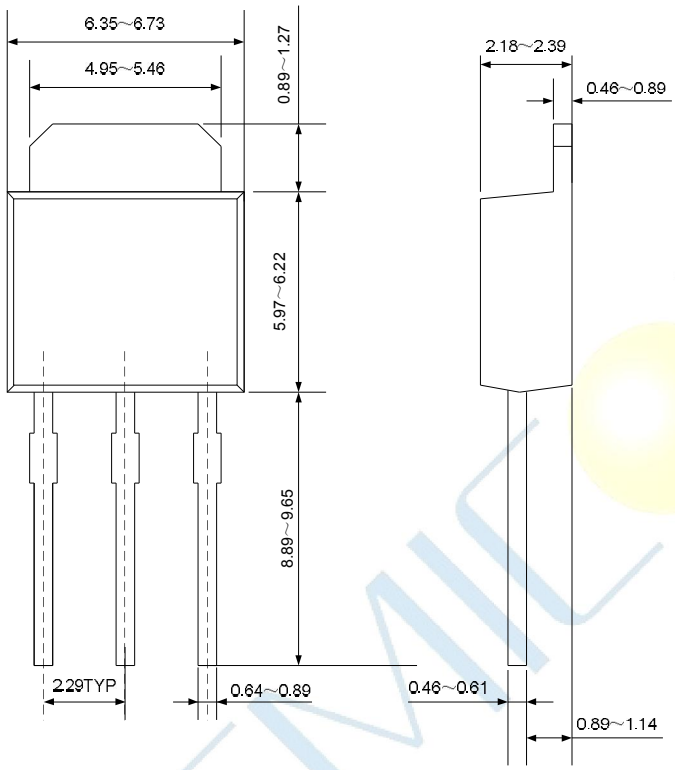
TO-252-2L **UNIT: mm**



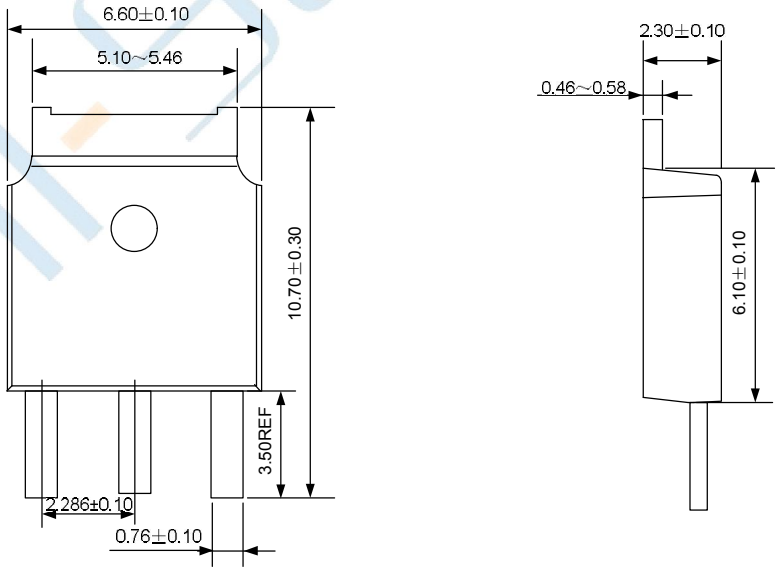
NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

PACKAGE OUTLINE (continued)

TO-251J-3L **UNIT: mm**



TO-251D-3L **UNIT: mm**



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