

1A, 600V N-CHANNEL MOSFET

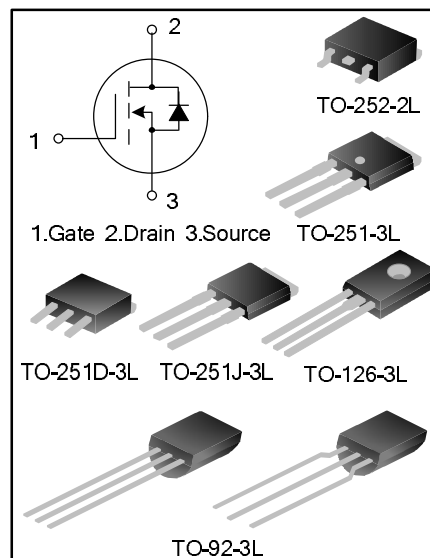
GENERAL DESCRIPTION

This power mosfet is an N-channel enhancement mode power MOS field effect transistor which is produced using Hi-semicon proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

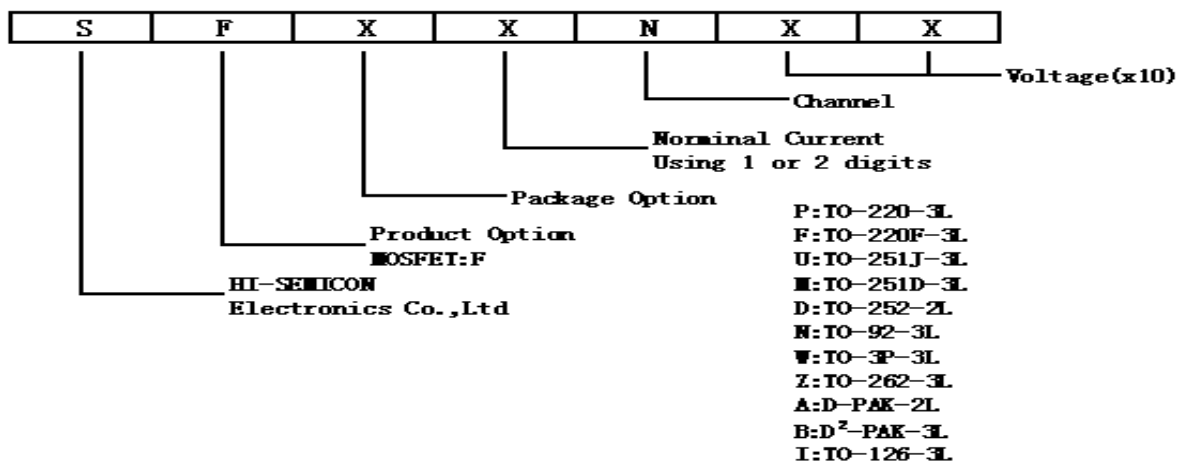
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- ◆ 1A, 600V, $R_{DS(on)}$ (typ.) = $8.2\Omega @ V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low C_{rss}
- ◆ Fast switching
- ◆ Improved dv/dt capability



NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SFM1N60	TO-251D-3L	SFM1N60	Pb free	Tube
SFU1N60	TO-251J-3L	SFU1N60	Pb free	Tube
SFI1N60	TO-126-3L	SFI1N60	Pb free	Bulk
SFN1N60	TO-92-3L	SFN1N60	Pb free	Bulk
SFN1N60TR	TO-92-3L	SFN1N60	Pb free	AMMO
SFD1N60	TO-252-2L	SFD1N60	Pb free	Tape & Reel

ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Characteristics		Symbol	Rating				Unit
			SFN1N60	SFM/D1N60	SFU1N60	SFI1N60	
Drain-Source Voltage		V _{DS}	600				V
Gate-Source Voltage		V _{GS}	±30				V
Drain Current	T _C =25°C	I _D	1.0				A
	T _C =100°C		0.63				
Drain Current Pulsed		I _{DM}	1.5	4.0			A
Power Dissipation(T _C =25°C) -Derate above 25°C		P _D	9	28	29	25	W
			0.07	0.22	0.23	0.20	W/°C
Single Pulsed Avalanche Energy (Note 1)		E _{AS}	52				mJ
Operation Junction Temperature Range		T _J	-55~+150				°C
Storage Temperature Range		T _{sta}	-55~+150				°C

THERMAL CHARACTERISTICS

Characteristics		Symbol	Rating				Unit
			SFN1N60	SFM/D1N60	SFU1N60	SF1N60	
Thermal Resistance, Junction-to-Case		R _{θJC}	13.89	4.46	4.31	5	°C/W
Thermal Resistance, Junction-to-Ambient		R _{θJA}	120	110	110	62.5	°C/W

ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B _{VDS}	V _{GS} =0V, I _D =250μA	600	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V	--	--	1.0	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} =V _{DS} , I _D =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =0.5 A	--	8.2	11	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHZ	--	120.3	--	pF
Output Capacitance	C _{oss}		--	19.0	--	
Reverse Transfer Capacitance	C _{rss}		--	0.8	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =300V, I _D =1.0A, R _G =25Ω (Note 2,3)	--	6.47	--	ns
Turn-on Rise Time	t _r		--	13.27	--	
Turn-off Delay Time	t _{d(off)}		--	7.73	--	
Turn-off Fall Time	t _f		--	15.87	--	
Total Gate Charge	Q _g	V _{DS} =480V, I _D =1.0A, V _{GS} =10V (Note 2,3)	--	3.45	--	nC
Gate-Source Charge	Q _{gs}		--	1.10	--	
Gate-Drain Charge	Q _{gd}		--	1.39	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.		Unit
					SFN1N60	Others	
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	1.0		A
Pulsed Source Current	I_{SM}		--	--	1.5	4.0	
Diode Forward Voltage	V_{SD}	$I_S=1.0A$, $V_{GS}=0V$	--	--	1.5		V
Reverse Recovery Time	T_{rr}	$I_S=1.0A$, $V_{GS}=0V$,	--	246.08	--		ns
Reverse Recovery Charge	Q_{rr}	$dI/dt=100A/\mu S$ (Note 2)	--	0.53	--		μC

Notes:

1. $L=30mH$, $I_{AS}=1.74A$, $V_{DD}=85V$, $R_G=25\Omega$, starting $T_J=25^\circ C$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycles $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

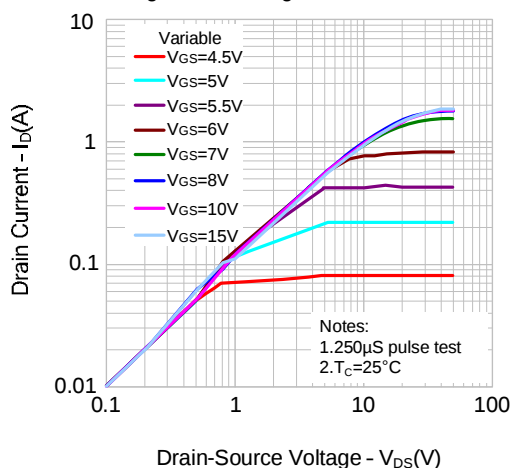


Figure 2. Transfer Characteristics

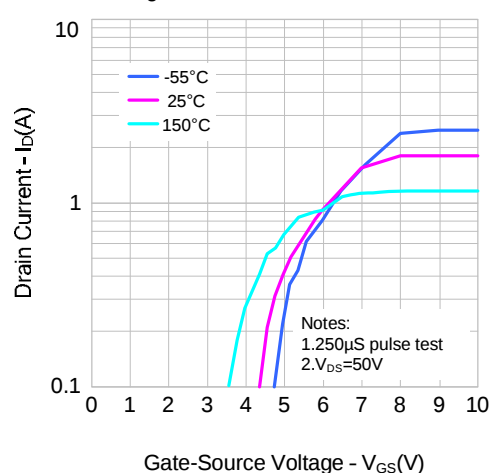


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

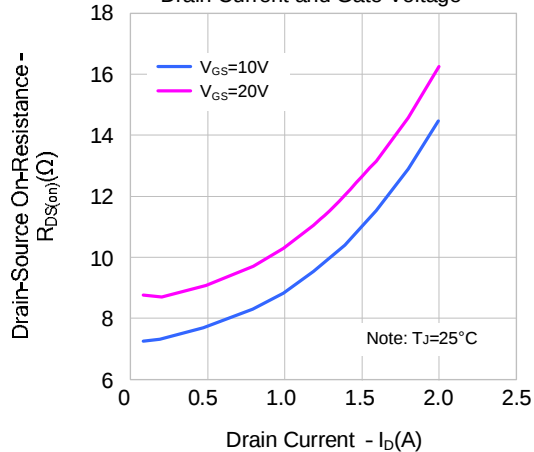
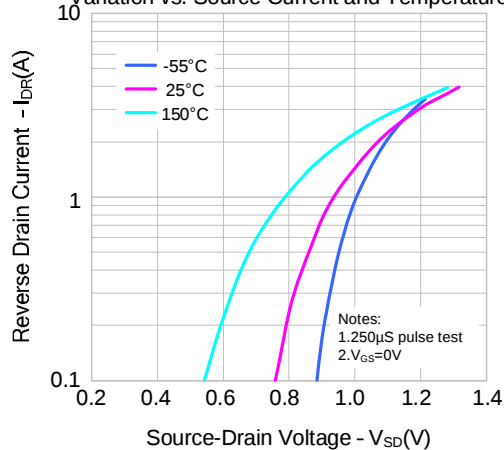


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL CHARACTERISTICS (continued)

Figure 5. Capacitance Characteristics

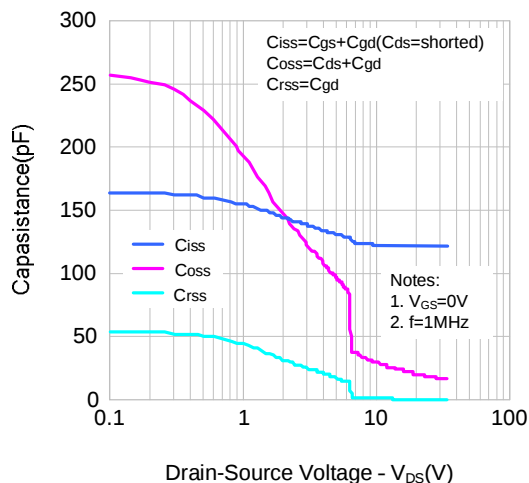


Figure 6. Gate Charge Characteristics

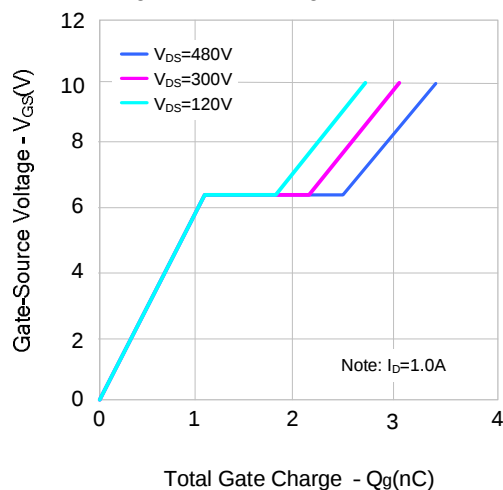


Figure 7. Breakdown Voltage Variation vs. Temperature

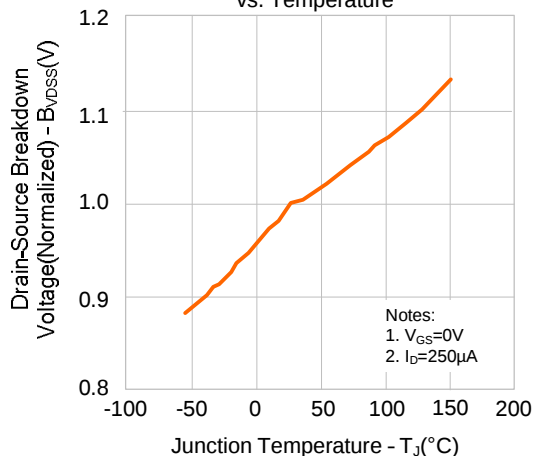


Figure 8. On-resistance Variation vs. Temperature

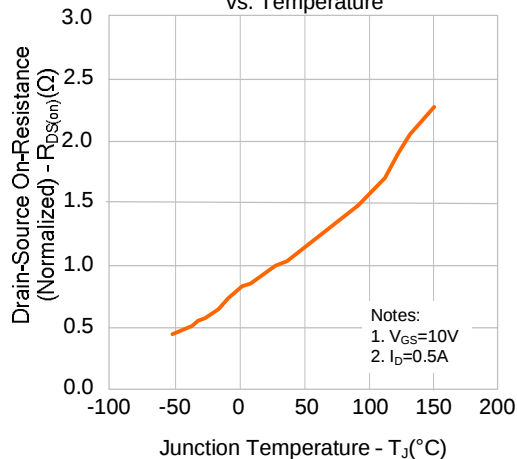


Figure 9-1. Max. Safe Operating Area (SFN1N60)

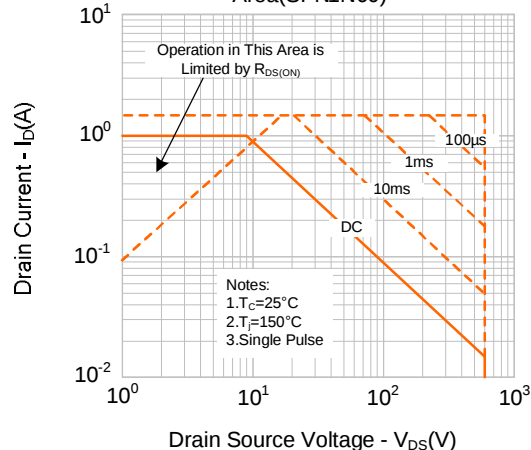
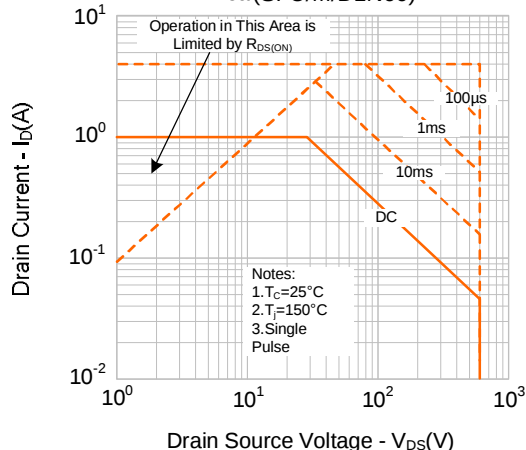
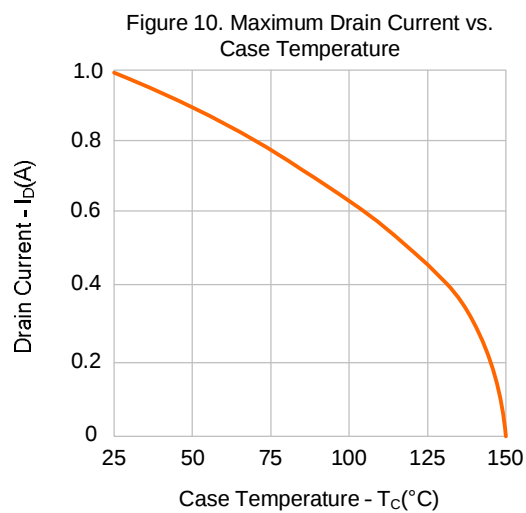
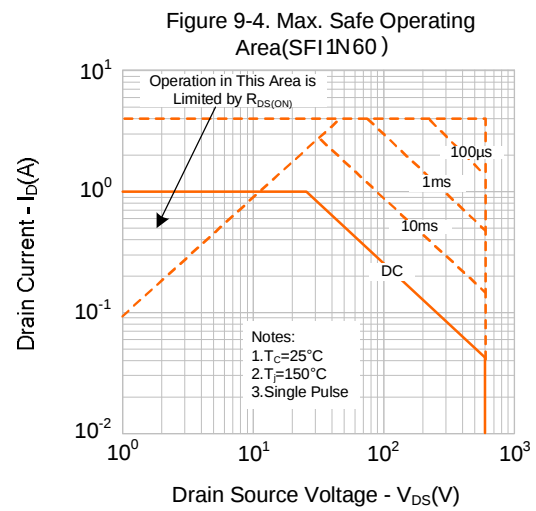
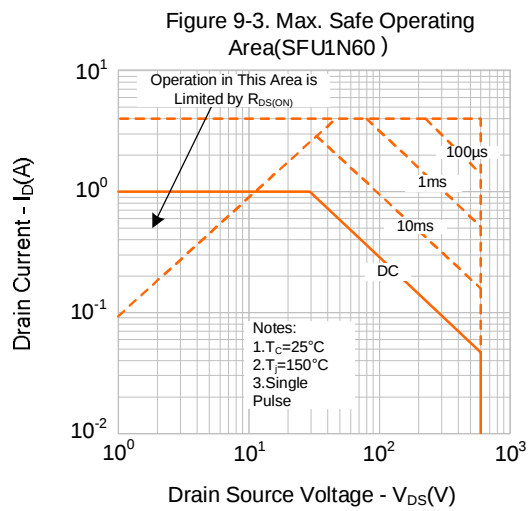


Figure 9-2. Max. Safe Operating Area (SFU/M/D1N60)

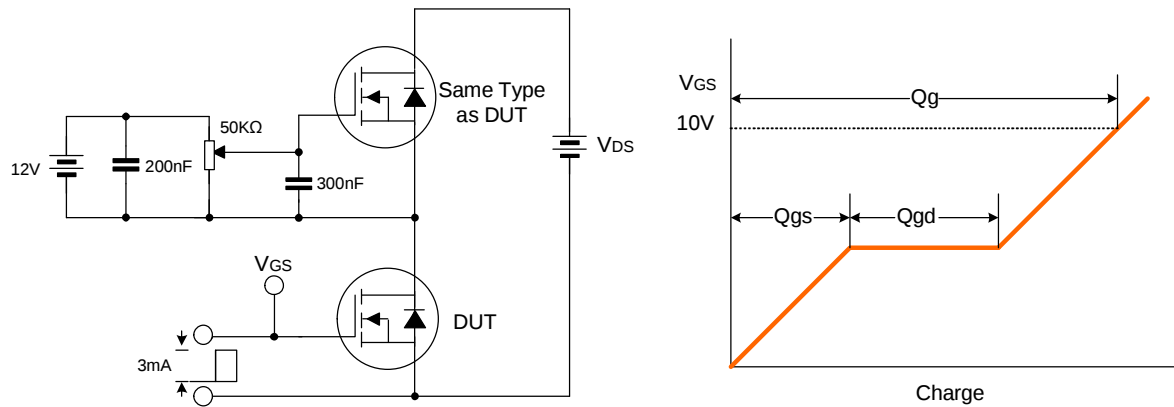


TYPICAL CHARACTERISTICS (continued)

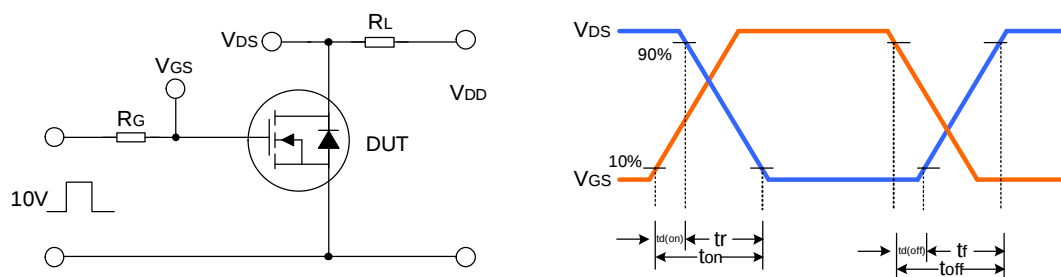


TYPICAL TEST CIRCUIT

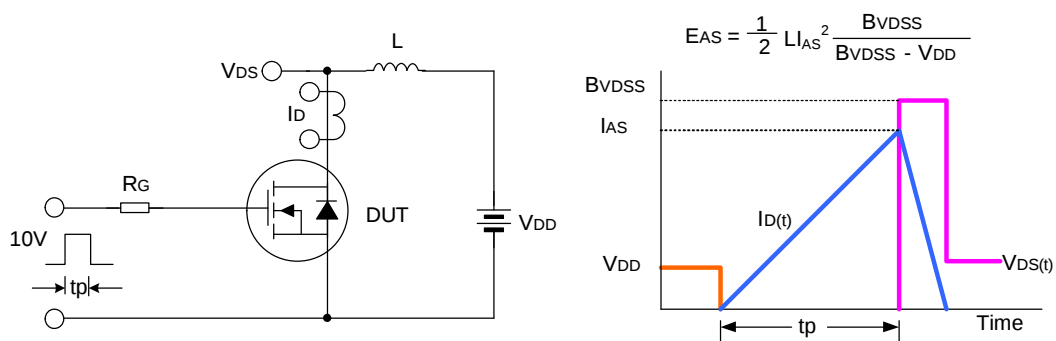
Gate Charge Test Circuit & Waveform



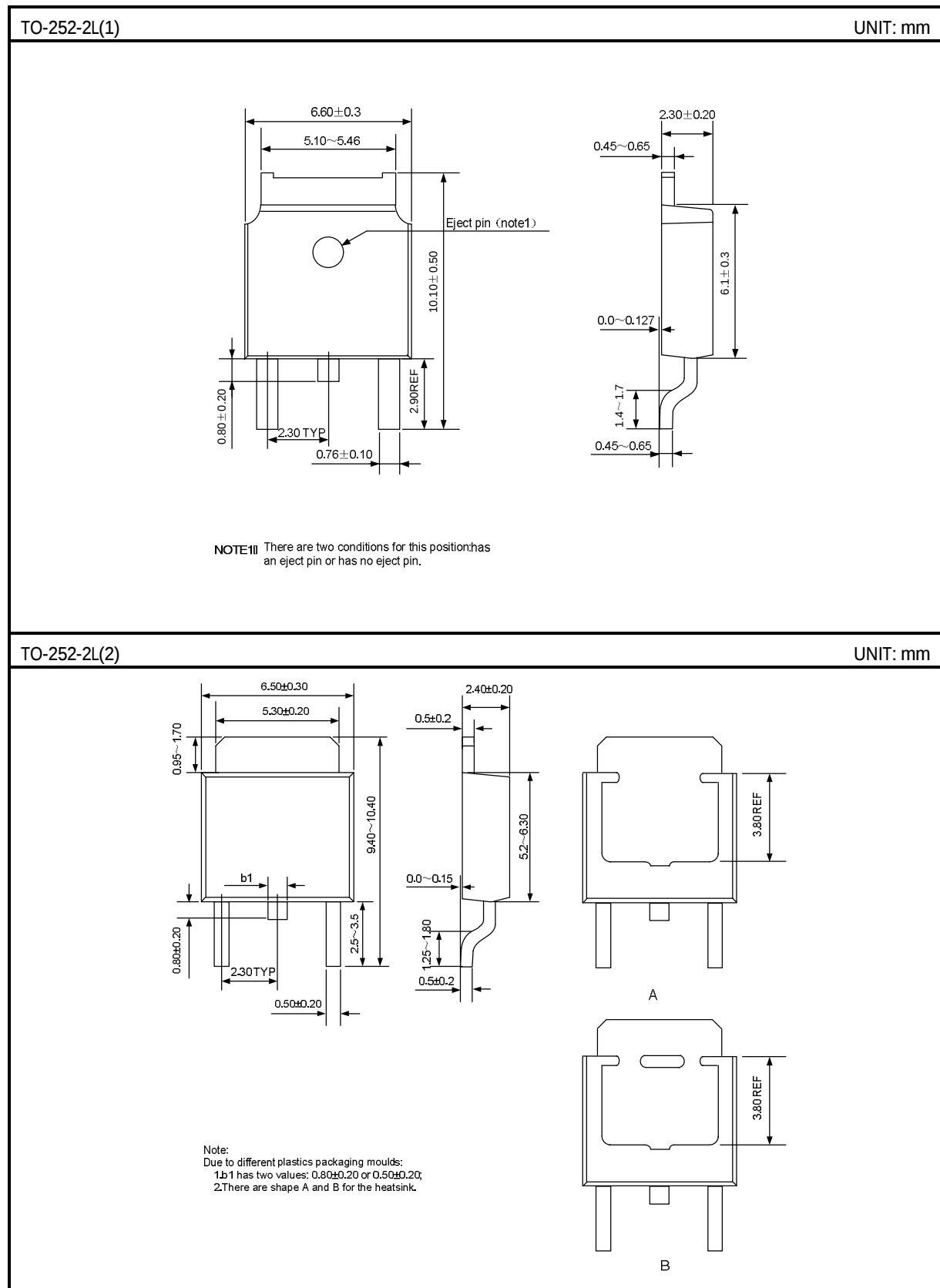
Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform



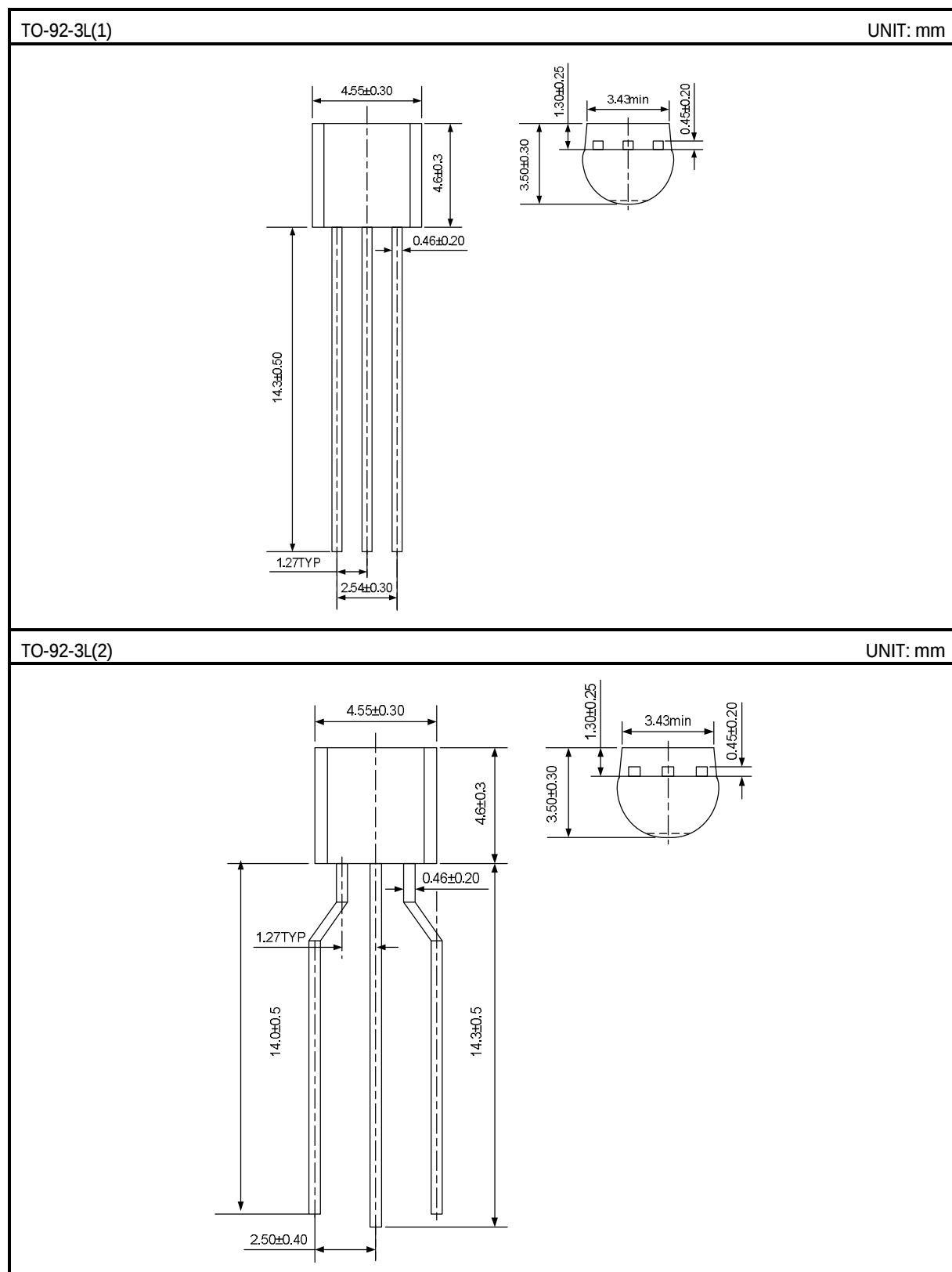
PACKAGE OUTLINE



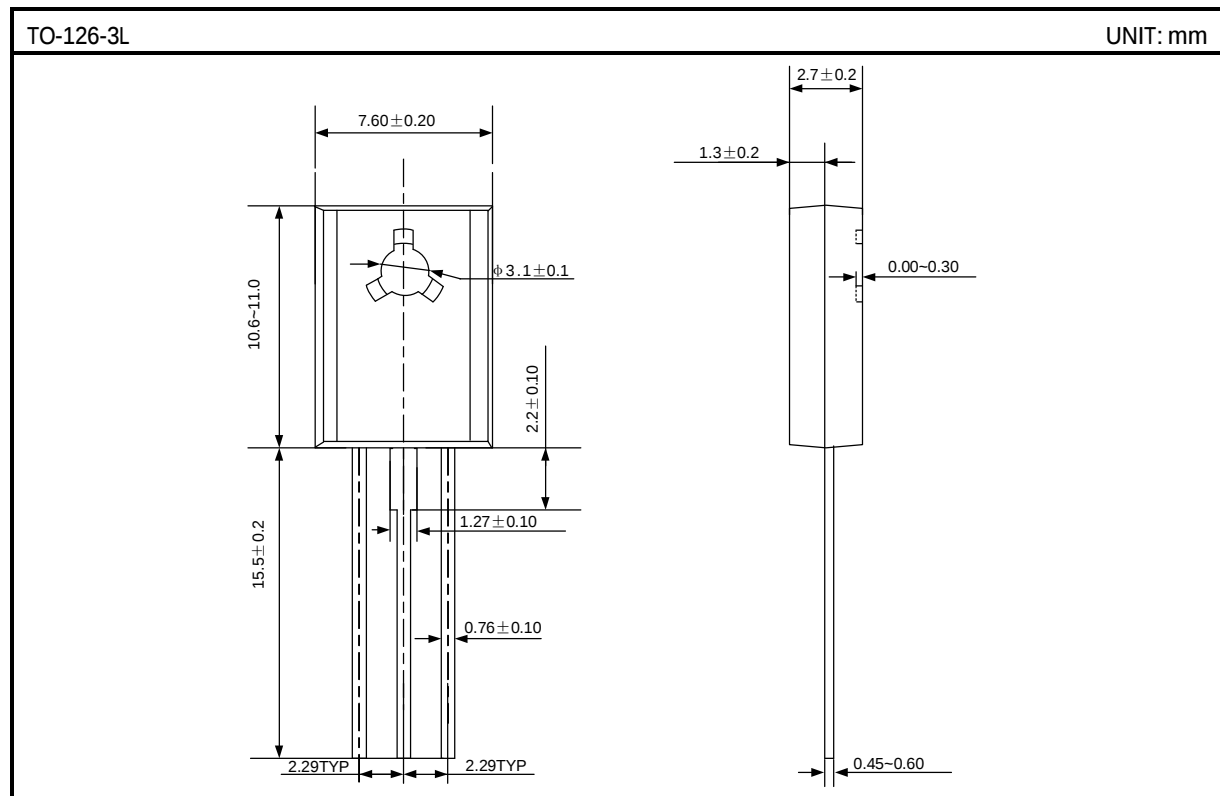
PACKAGE OUTLINE (continued)

TO-251J-3L	UNIT: mm
Technical drawing of the TO-251J-3L package. The top view shows a rectangular body with a central square area. Dimensions include: overall width 6.35~6.73, inner width 4.95~5.46, height 0.89~1.27, body height 5.97~6.22, and a central square area with side length 8.89~9.65. The side view shows a rectangular body with a central square area. Dimensions include: overall width 2.18~2.39, inner width 0.46~0.89, body height 0.46~0.61, and a central square area with side length 0.89~1.14. The bottom view shows three pins with dimensions: pin width 2.29TYP, pin spacing 0.64~0.89, and pin height 0.46~0.61.	
TO-251D-3L	UNIT: mm
Technical drawing of the TO-251D-3L package. The top view shows a rectangular body with a central square area. Dimensions include: overall width 6.60±0.10, inner width 5.10~5.46, height 10.70±0.30, and a central square area with side length 3.50REF. The side view shows a rectangular body with a central square area. Dimensions include: overall width 2.30±0.10, inner width 0.46~0.58, body height 6.10±0.10, and a central square area with side length 0.76±0.10. The bottom view shows three pins with dimensions: pin width 2.286±0.10, pin spacing 0.76±0.10, and pin height 3.50REF.	

PACKAGE OUTLINE (continued)



PACKAGE OUTLINE (continued)



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