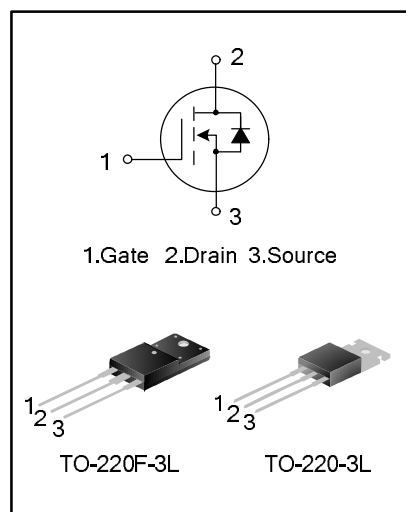


10A, 650V N-CHANNEL MOSFET

GENERAL DESCRIPTION

This power mosfet is an N-channel enhancement mode power MOS field effect transistor which is produced using Hi-semicon proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

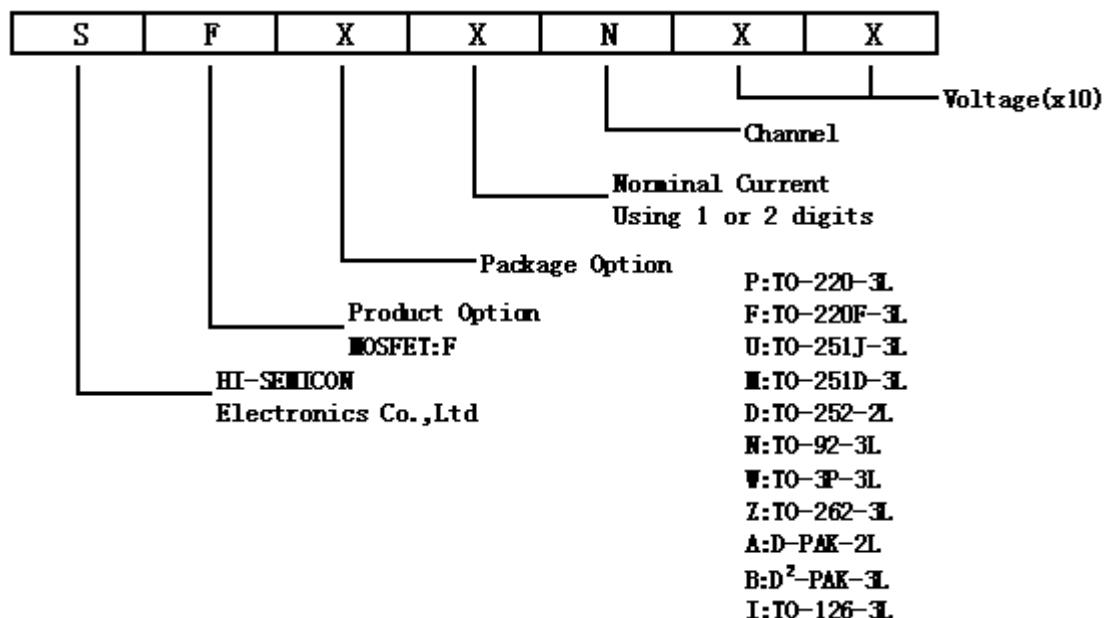
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- ◆ 10A, 650V, $R_{DS(on)}(typ.) = 0.80\Omega @ V_{GS} = 10V$
- ◆ Low gate charge
- ◆ Low C_{rss}
- ◆ Fast switching
- ◆ Improved dv/dt capability

NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SFP10N65	TO-220-3L	SFP10N65	Pb free	Tube
SFF10N65	TO-220F-3L	SFF10N65	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Characteristics		Symbol	Ratings		Unit
			SFP10N65	SFF10N65F	
Drain-Source Voltage		V _{DS}	650		V
Gate-Source Voltage		V _{GS}	±30		V
Drain Current	T _C = 25°C	I _D	10		A
	T _C = 100°C		5.5		
Drain Current Pulsed		I _{DM}	40		A
Power Dissipation(T _C =25°C) -Derate above 25°C		P _D	156	50	W
			1.25	0.4	W/°C
Single Pulsed Avalanche Energy (Note 1)		E _{AS}	608		mJ
Operation Junction Temperature Range		T _J	-55~+150		°C
Storage Temperature Range		T _{stg}	-55~+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SFP10N65	SFF10N65	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.8	2.5	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	120	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$B_{V_{DS}}$	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=650\text{V}, V_{GS}=0\text{V}$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30\text{V}, V_{DS}=0\text{V}$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=5.0\text{A}$	--	0.8	1.0	Ω
Input Capacitance	C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0\text{V},$ $f=1.0\text{MHZ}$	--	1143.2	--	pF
Output Capacitance	C_{oss}		--	128.8	--	
Reverse Transfer Capacitance	C_{rss}		--	3.5	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=325\text{V}, I_D=10\text{A},$ $R_G=25\Omega$ (Note 2,3)	--	40.00	--	ns
Turn-on Rise Time	t_r		--	73.67	--	
Turn-off Delay Time	$t_{d(off)}$		--	52.13	--	
Turn-off Fall Time	t_f		--	34.80	--	
Total Gate Charge	Q_g	$V_{DS}=520\text{V}, I_D=10\text{A},$ $V_{GS}=10\text{V}$ (Note 2,3)	--	20.00	--	nC
Gate-Source Charge	Q_{gs}		--	7.47	--	
Gate-Drain Charge	Q_{gd}		--	6.48	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse p-n Junction Diode in the MOSFET	--	--	10	A
Pulsed Source Current	I_{SM}		--	--	40	
Diode Forward Voltage	V_{SD}	$I_S=10A, V_{GS}=0V$	--	--	1.3	V
Reverse Recovery Time	T_{rr}	$I_S=10A, V_{GS}=0V,$ $dI_F/dt=100A/\mu S$	--	570.8	--	ns
Reverse Recovery Charge	Q_{rr}		--	4.71	--	μC

Notes:

1. $L=30mH, I_{AS}=5.82A, V_{DD}=150V, R_G=25\Omega$, starting $T_J=25^\circ C$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycles $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

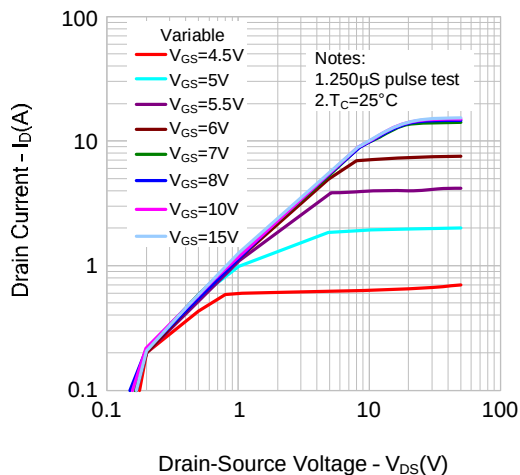


Figure 2. Transfer Characteristics

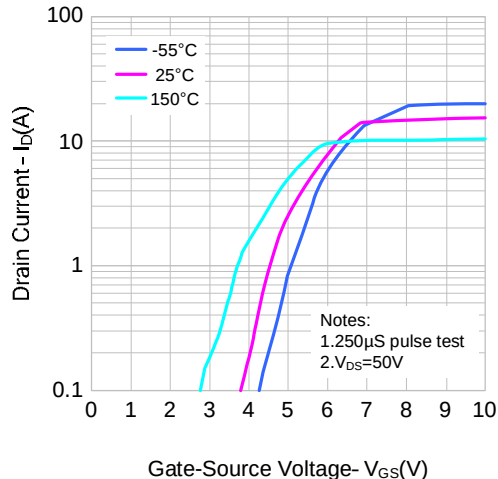


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

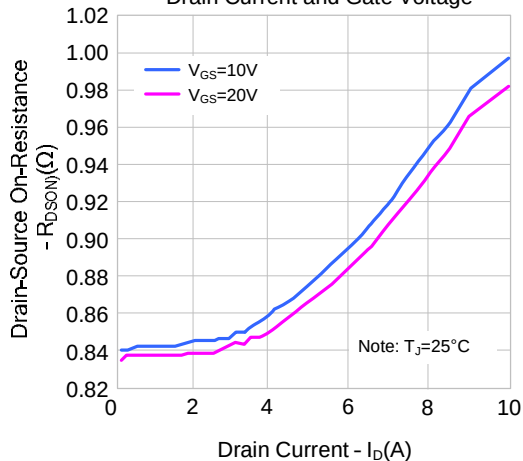


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

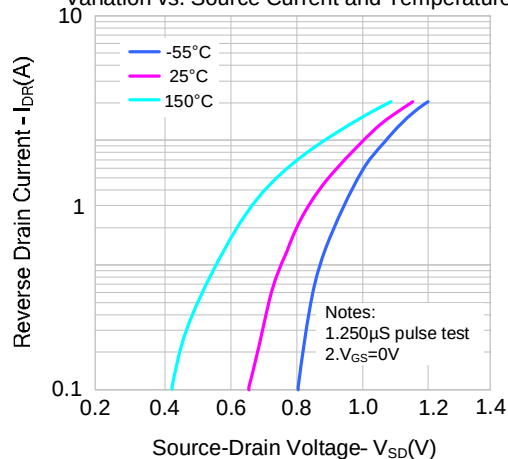


Figure 5. Capacitance Characteristics

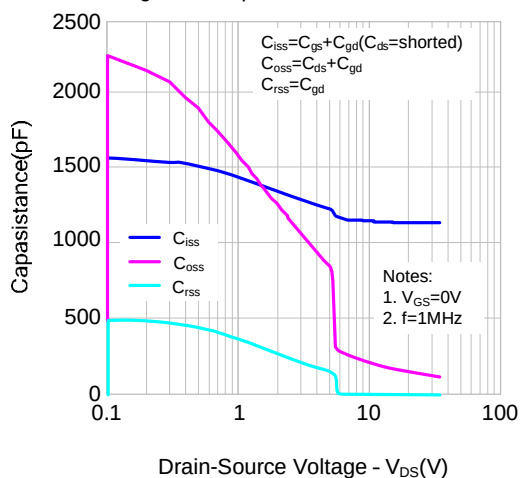
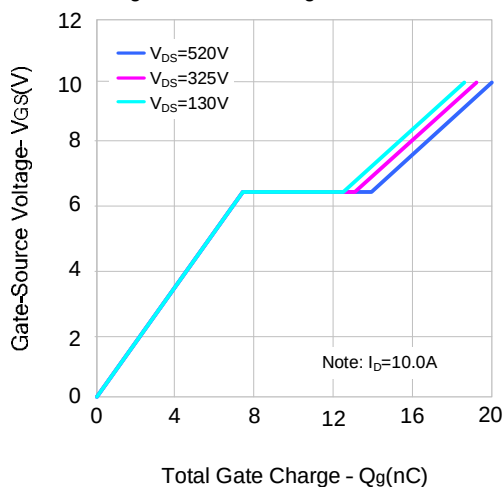


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS (continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

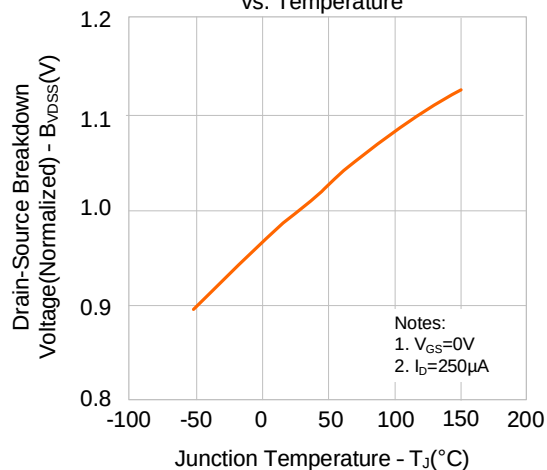


Figure 8. On-resistance Variation vs. Temperature

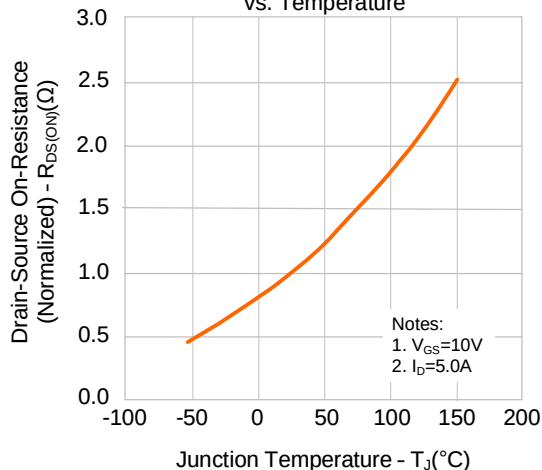


Figure 9-1. Max. Safe Operating Area (SFP10N65)

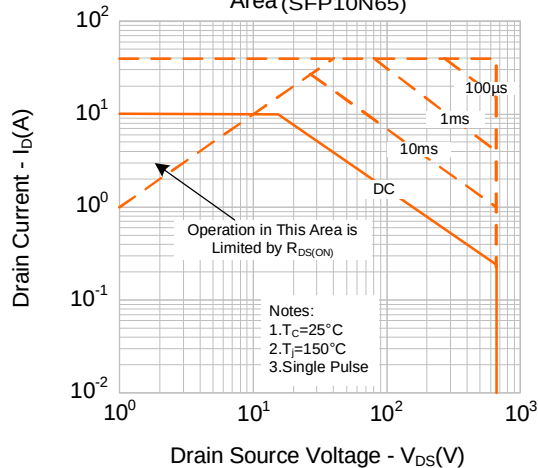


Figure 9-2. Max. Safe Operating Area (SFF10N65)

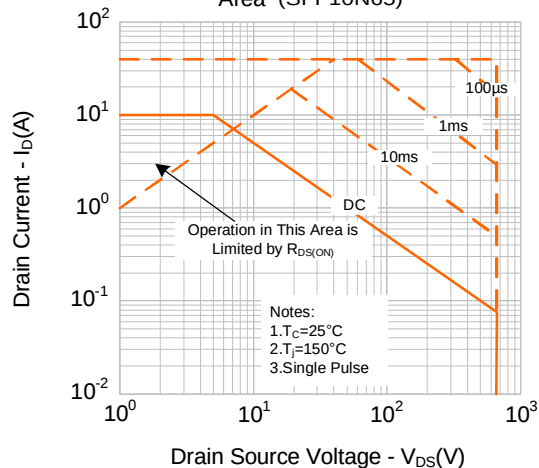
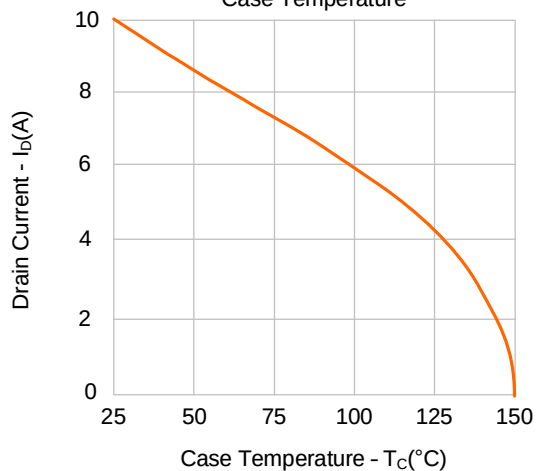
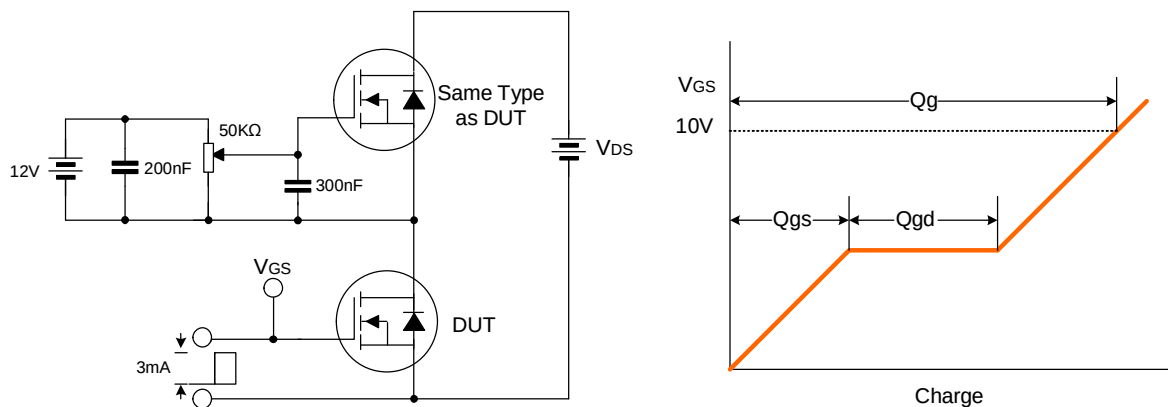


Figure 10. Maximum Drain Current vs. Case Temperature

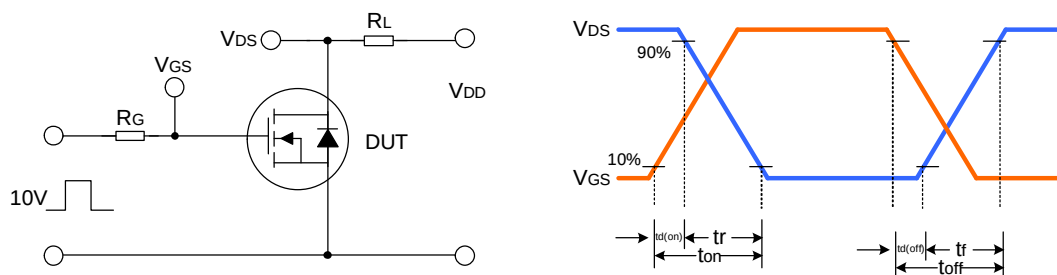


TYPICAL TEST CIRCUIT

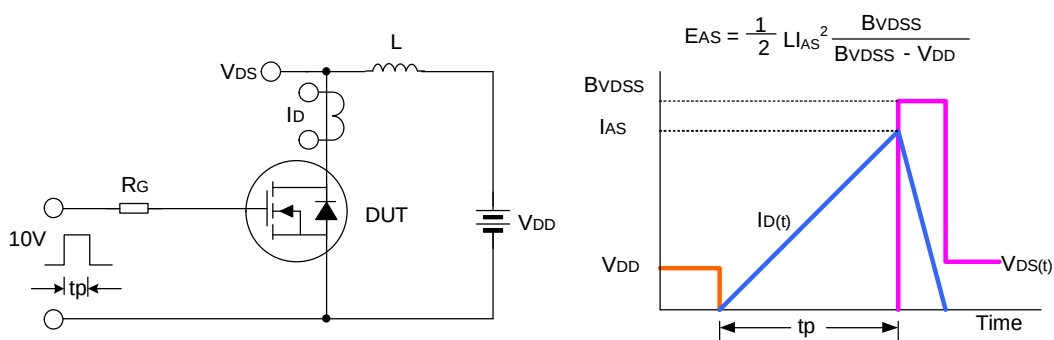
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



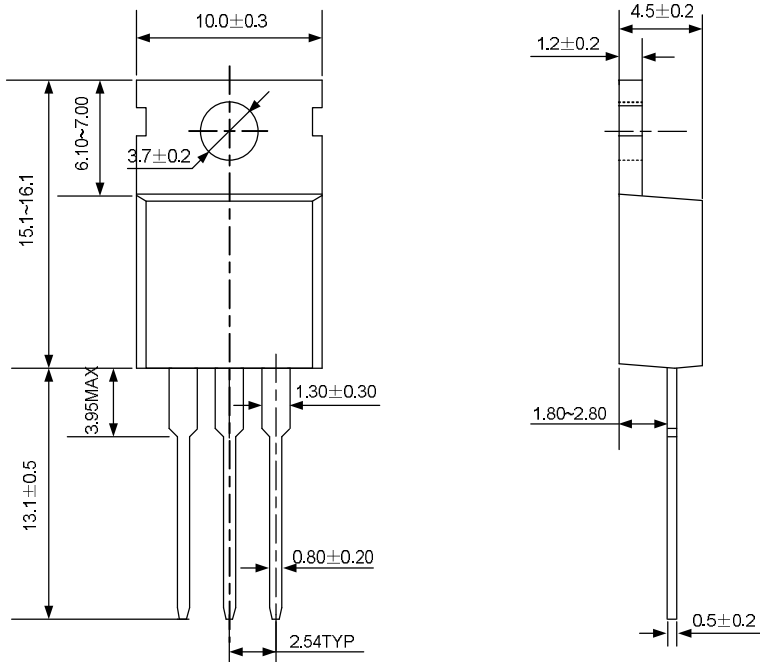
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

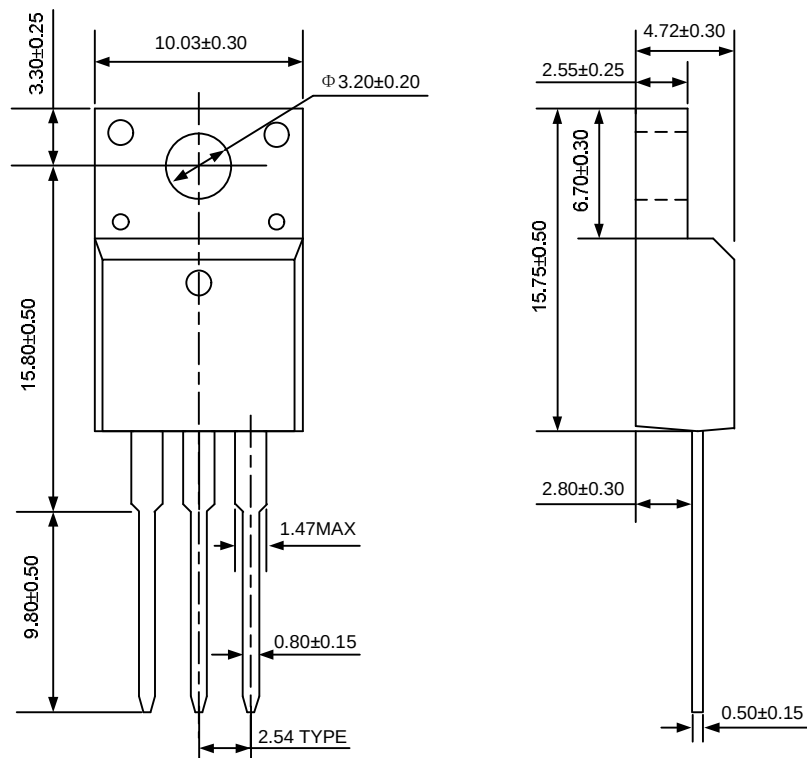
TO-220-3L

UNIT: mm



TO-220F-3L

UNIT: mm



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