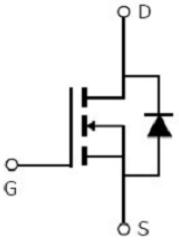
Main Product Characteristics:

V_{DSS}	60V
R_{DS}(on)	7.2mohm(typ.)
I_D	110A

TO220

Marking and pin Assignment



Schematic diagram

Features and Benefits:

- Advanced Process Technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175℃ operating temperature

Description:

These N-Channel enhancement mode power field effect transistors are produced using silikron proprietary MOSFET technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V①	110	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS}@ 10V①	83	
I_{DM}	Pulsed Drain Current②	440	
P_D @TC = 25°C	Power Dissipation③	200	W
	Linear Derating Factor	1.3	W/°C
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ L=0.3mH	576	mJ
I_{AS}	Avalanche Current @ L=0.3mH	62	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C

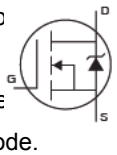
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case③	—	0.75	℃/W
$R_{\theta JA}$	Junction-to-ambient (t ≤ 10s) ④	—	62	℃/W
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	40	℃/W

Electrical Characterizes @T_A=25℃ unless otherwise specified

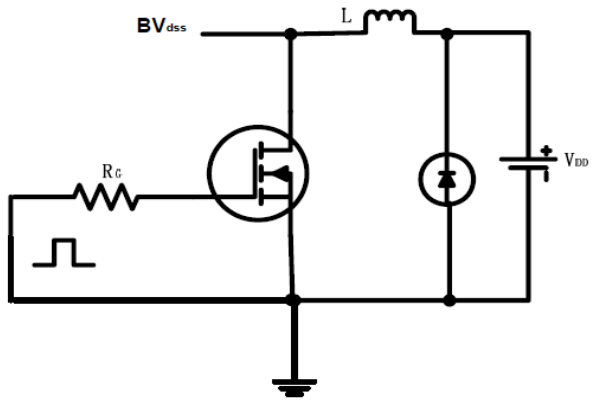
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	55	—	—	V	V_{GS} = 0V, ID = 250μA
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	7.2	8	mΩ	V_{GS}=10V,I_D =62A
		—	12.7	—		T_J = 125℃
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	V_{DS} = V_{GS}, I_D = 250μA
		—	2.2	—		T_J = 125℃
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	V_{DS} = 55V,V_{GS} = 0V
		—	—	50		T_J = 125°C
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V_{GS} =20V
		-100	—	—		V_{GS} = -20V
Q_g	Total gate charge	51	57	63	nC	I_D = 62A,
Q_{gs}	Gate-to-Source charge	—	7	—		V_{DS}=44V,
Q_{gd}	Gate-to-Drain("Miller") charge	—	34.5	—		V_{GS} = 10V
$t_{d(on)}$	Turn-on delay time	—	16.2	—	ns	V_{GS}=10V, VDD=29.1V,
t_r	Rise time	—	90.0	—		R_L=0.47Ω,
$t_{d(off)}$	Turn-Off delay time	—	33.8	—		R_{GEN}=4.5Ω
t_f	Fall time	—	18.3	—		ID=62A
C_{iss}	Input capacitance	—	3014	—	pF	V_{GS} = 0V
C_{oss}	Output capacitance	—	721	—		V_{DS} = 25V
C_{rss}	Reverse transfer capacitance	—	113	—		f = 1MHz

Source-Drain Ratings and Characteristics

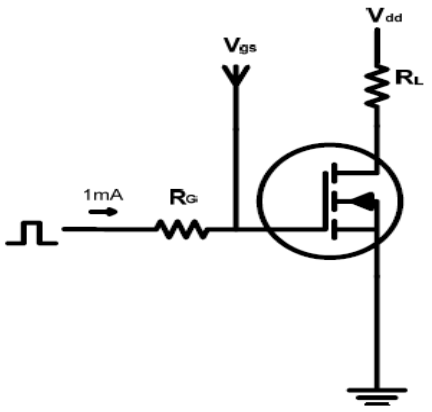
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	110	A	MOSFET symb showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	440	A	
V_{sd}	Diode Forward Voltage	—	0.88	1.5	V	I_S=62A, V_{GS}=0V, T_J = 25°C
t_{rr}	Reverse Recovery Time	—	42	—	ns	T_J = 25°C, I_F =62A, di/dt = 100A/μs
Q_{rr}	Reverse Recovery Charge	—	62	—	nC	

Test circuits and Waveforms

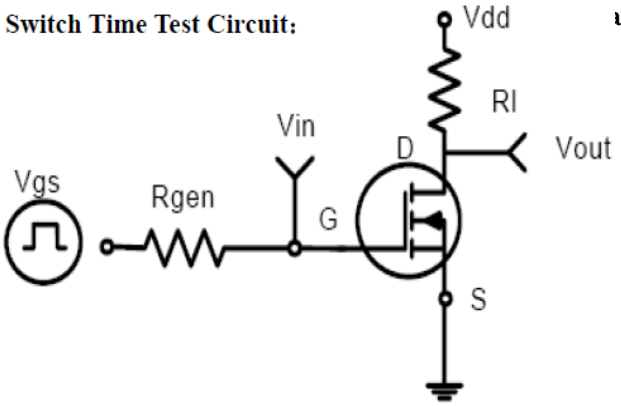
EAS test circuits:



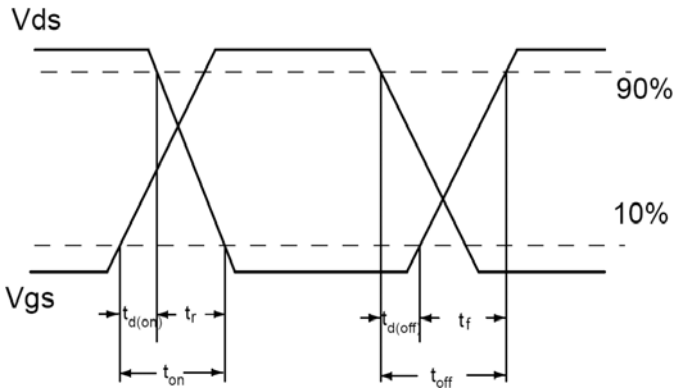
Gate charge test circuit:



Switch Time Test Circuit:



ıveforms:



Notes:

①The maximum current rating is limited by bond-wires.
②Repetitive rating; pulse width limited by max. junction temperature.
③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
④The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C
⑤These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.
⑥ The maximum current rating is limited by bond-wires.

Typical electrical and thermal characteristics

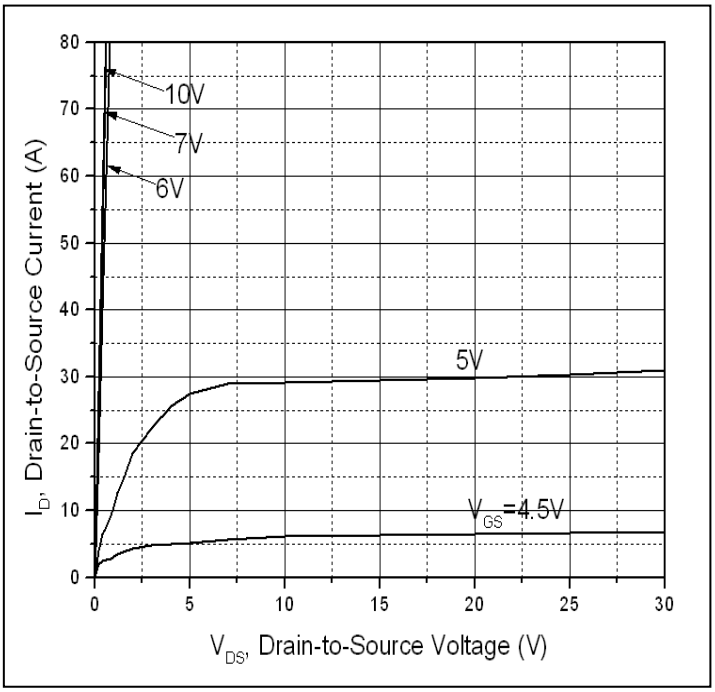


Figure 1: Typical Output Characteristics

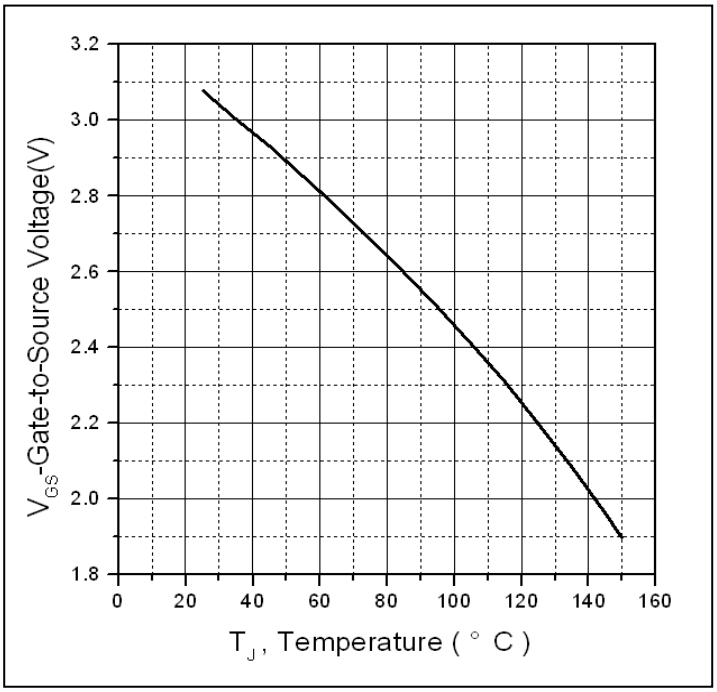


Figure 2. Gate to source cut-off voltage

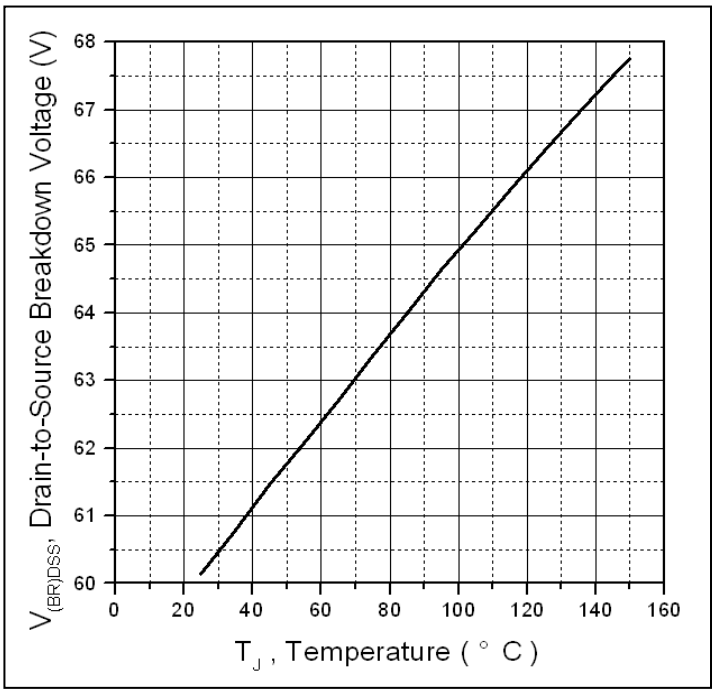


Figure 3. Drain-to-Source Breakdown Voltage vs. Temperature

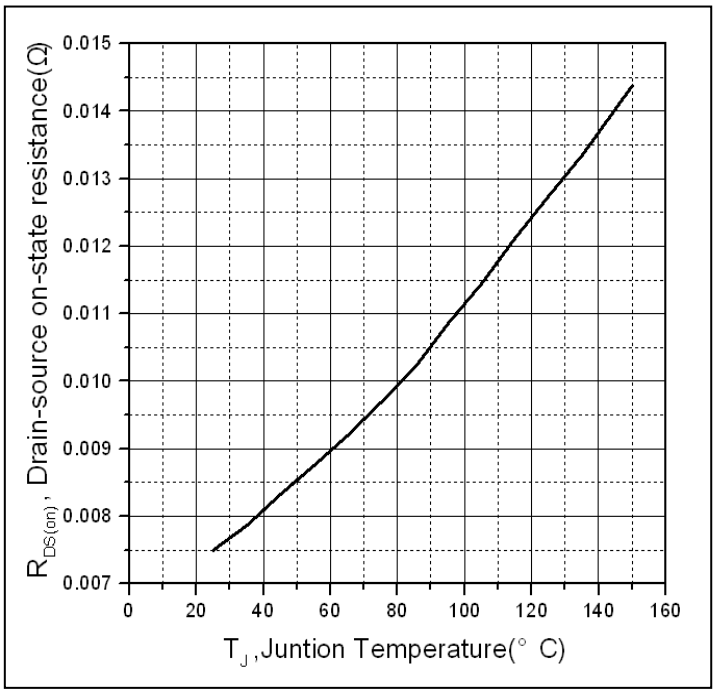


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

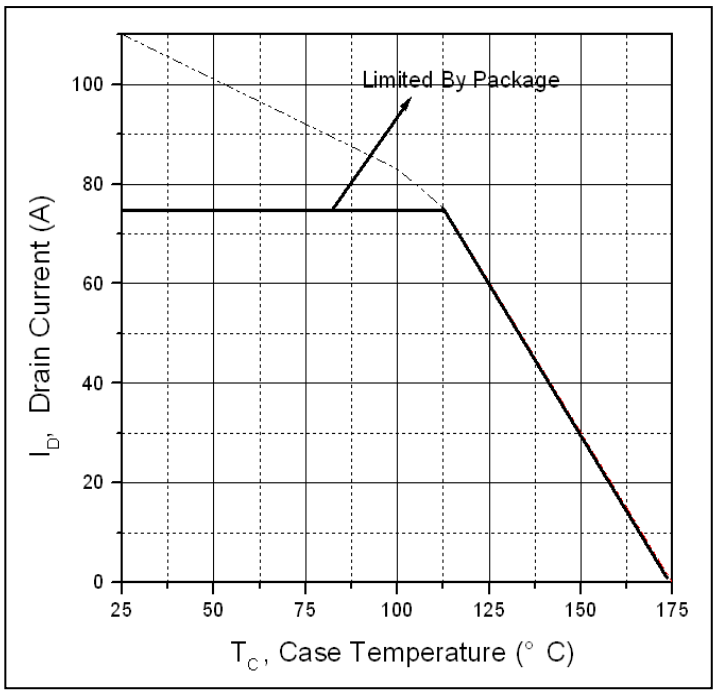


Figure 5. Maximum Drain Current Vs. Case Temperature

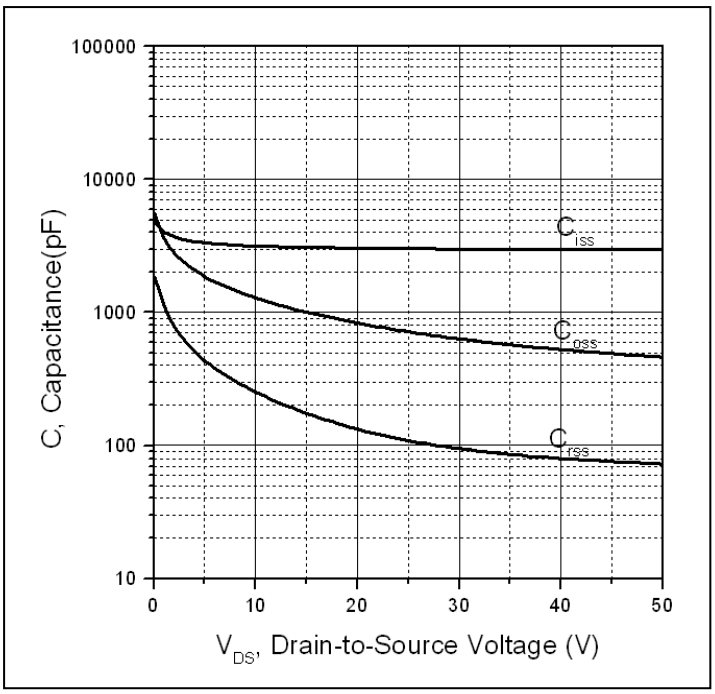


Figure 6.Typical Capacitance Vs. Drain-to-Source Voltage

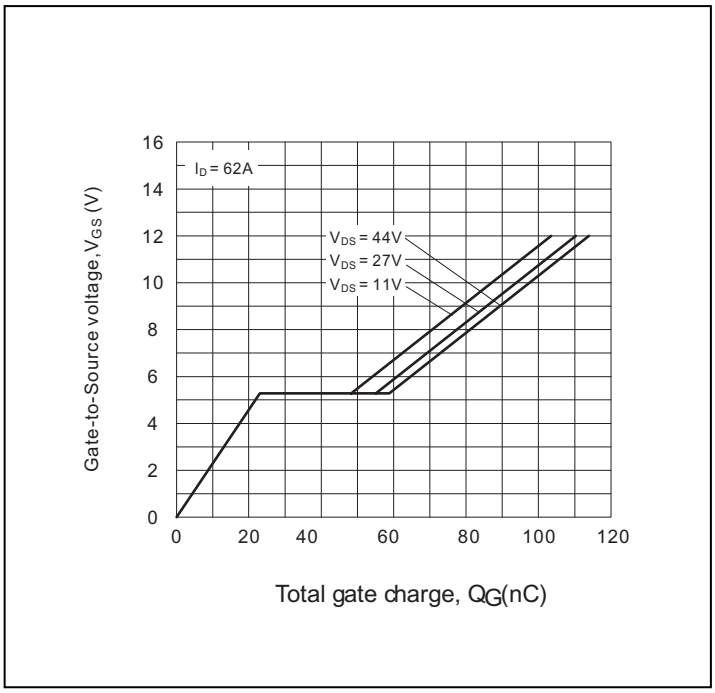


Fig.7 Typical gate charge vs. Gate-to-Source voltage

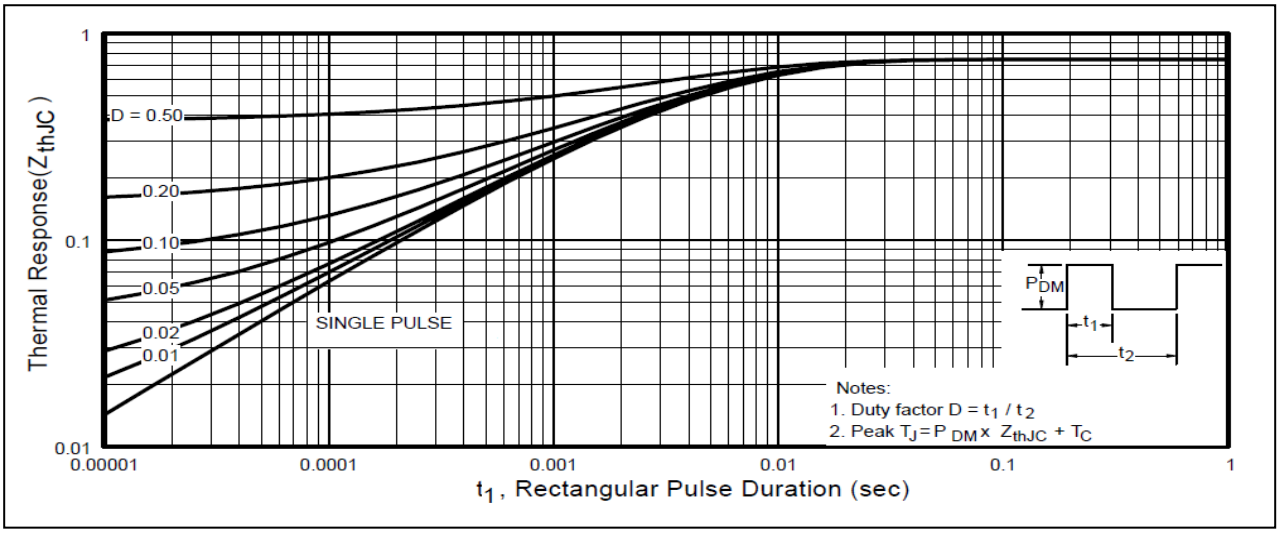
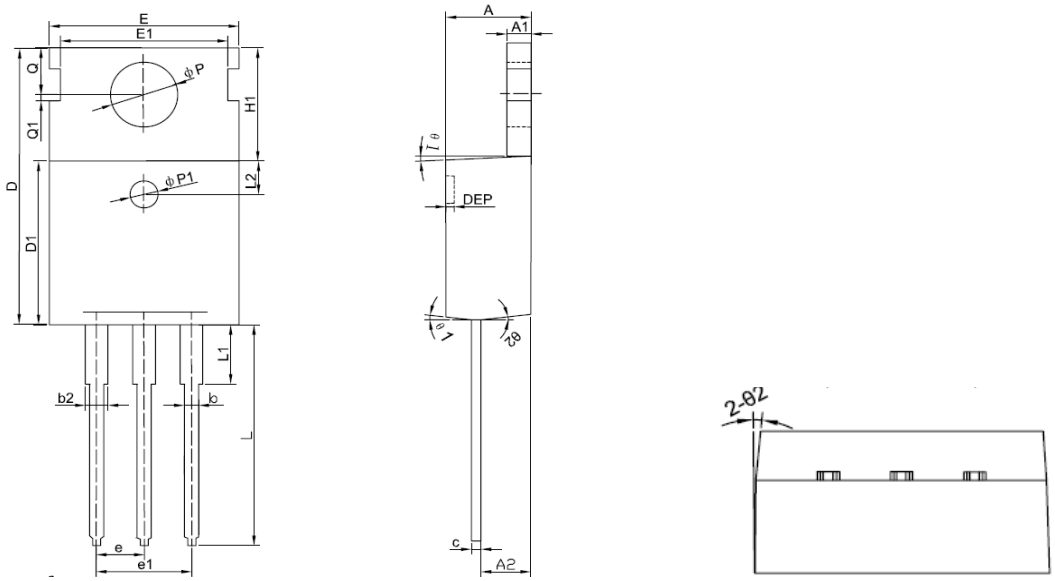


Figure8. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data：

TO220 PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.400	4.550	4.700	0.173	0.179	0.185
A1	1.270	1.300	1.330	0.050	0.051	0.052
A2	2.590	2.690	2.790	0.102	0.106	0.110
b	0.770	-	0.900	0.030	-	0.035
b2	1.230	-	1.360	0.048	-	0.054
c	0.480	0.500	0.520	0.019	0.020	0.020
D	15.100	15.400	15.700	-	0.606	-
D1	9.000	9.100	9.200	0.354	0.358	0.362
DEP	0.050	0.285	0.520	0.002	0.011	0.020
E	10.060	10.160	10.260	0.396	0.400	0.404
E1	-	8.700	-	-	0.343	-
ΦP1	1.400	1.500	1.600	0.055	0.059	0.063
e	2.54BSC			0.1BSC		
e1	5.08BSC			0.2BSC		
H1	6.100	6.300	6.500	0.240	0.248	0.256
L	12.750	12.960	13.170	0.502	0.510	0.519
L1	-	-	3.950	-	-	0.156
L2	1.85REF			0.073REF		
ΦP	3.570	3.600	3.630	0.141	0.142	0.143
Q	2.730	2.800	2.870	0.107	0.110	0.113
Q1	-	0.200	-	-	0.008	-
□1	5^0	7^0	9^0	5^0	7^0	9^0
□2	1^0	3^0	5^0	1^0	3^0	5^0

Ordering and Marking Information

Device Marking: SS110N06

Package (Available)

TO220

Operating Temperature Range

C : -55 to175 ºC

Devices per Unit

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO220	50	20	1000	6	6000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125℃ to 175℃ @ 80% of Max $V_{DSS}/V_{CES}/VR$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=125℃ or 175℃ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices