

COMPLEMENTARY HIGH-POWER SILICON POWER TRANSISTORS

Description

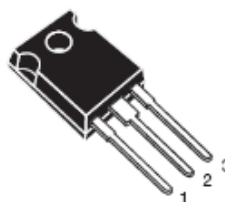
The devices are manufactured in planar technology with “base island” layout. The resulting transistors show exceptional high gain performance coupled with very low saturation voltage.

FEATURES

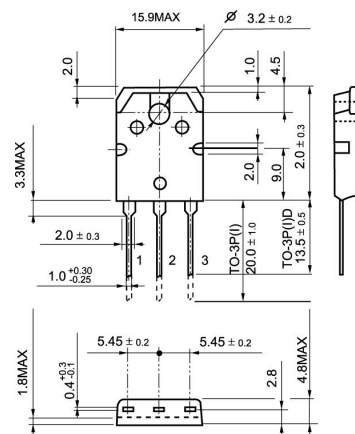
- Recommended for 75W Audio Frequency Amplifier Output Stage.
- Low collector-emitter saturation voltage
- I_{Cmax} :25A.
- Complementary NPN - PNP transistors

MAXIMUM RATINGS ($T_a=25^{\circ}\text{C}$)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Base Voltage	V_{CBO}	100	V
Collector-Emitter Voltage	V_{CEO}	100	V
Emitter-Base Voltage	V_{EB0}	5	V
Collector Current	I_C	25	A
Base Current	I_B	5.0	A
Collector Power Dissipation ($T_c=25^{\circ}\text{C}$)	P_C	125	W
Junction Temperature	T_j	150	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	$-55\sim 150$	$^{\circ}\text{C}$



TO-247



ELECTRICAL CHARACTERISTICS ($T_a=25^{\circ}\text{C}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current	I_{CBO}	$V_{CB}=100\text{V}, I_E=0$	-	-	10	μA
Emitter Cut-off Current	I_{EBO}	$V_{EB}=5\text{V}, I_C=0$	-	-	10	μA
Collector-emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C=50\text{mA}, I_B=0$	100	-	-	V
DC Current Gain	$h_{FE} 1$ (Note)	$V_{CE}=5\text{V}, I_C=1.5\text{A}$	55	-	160	
	$h_{FE} 2$	$V_{CE}=4\text{V}, I_C=15\text{A}$	15	-	-	
Collector-Emitter Saturation Voltage	$V_{CE(sat)} 1$	$I_C=15\text{A}, I_B=1.5\text{A}$	-	-	1.8	V
	$V_{CE(sat)} 2$	$I_C=25\text{A}, I_B=5.0\text{A}$	-	-	4.0	
Base-Emitter Voltage	V_{BE}	$V_{CE}=5\text{V}, I_C=5\text{A}$	-	-	1.5	V
Transition Frequency	f_T	$V_{CE}=5\text{V}, I_C=1\text{A}$	3.0	-	-	MHz

Note: h_{FE} Classification R:55~110, O:80~160

FIG-1 DC CURRENT GAIN

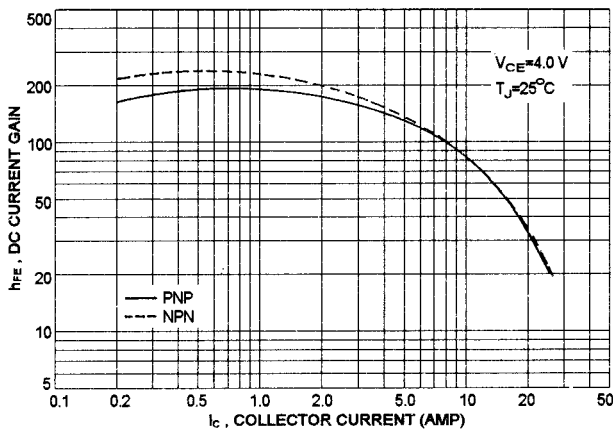


FIG-2 TURN-OFF TIME

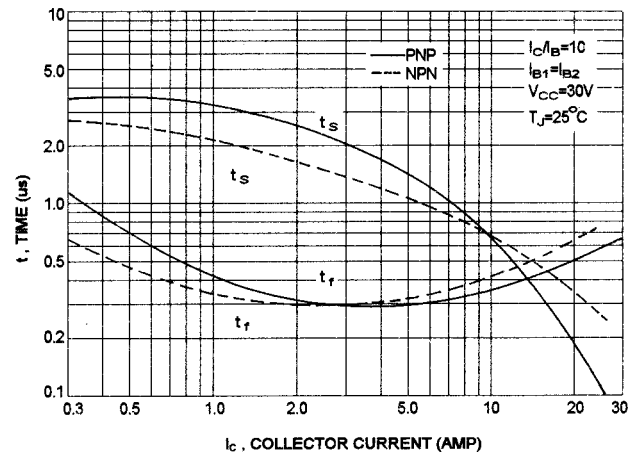


FIG-3 TURN-ON TIME

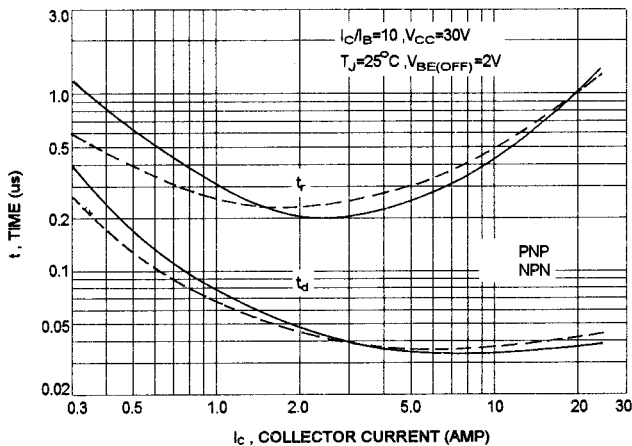


FIG-4 REVERSE BIASE SAFE OPERATING AREA

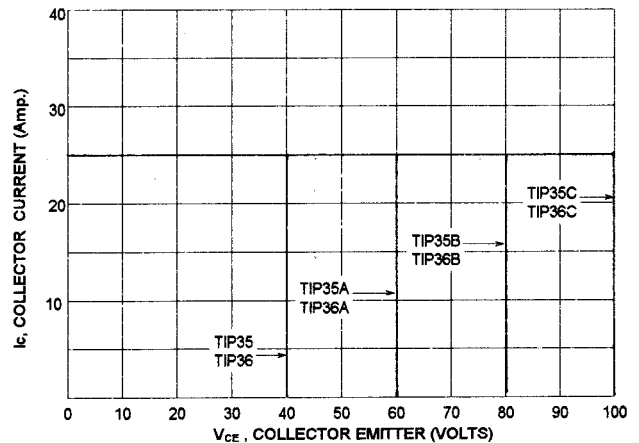
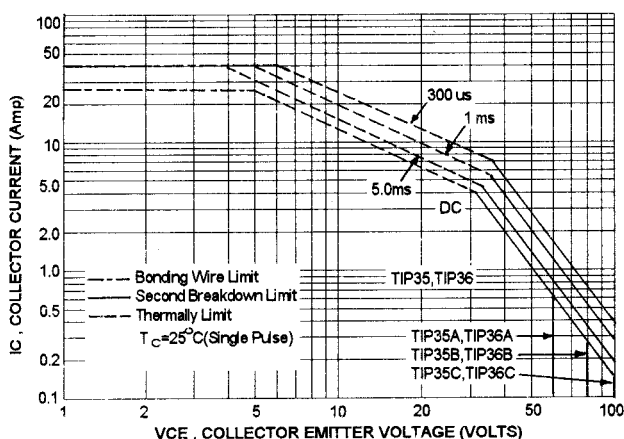


FIG-5 ACTIVE REGION SAFE OPERATING AREA



There are two limitation on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of FIG-6 is base on $T_C=25^\circ\text{C}$; $T_{J(PK)}$ is variable depending on power level. second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$, second breakdown limitations do not derate the same as thermal limitation.